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MOVES TRENCH ETCHING INTO THE FACTORY/75

MIDYEAR MARKET REPORT
PAGE 44

JULY 9, 1987

A McGRAW-HILL PUBLICATION

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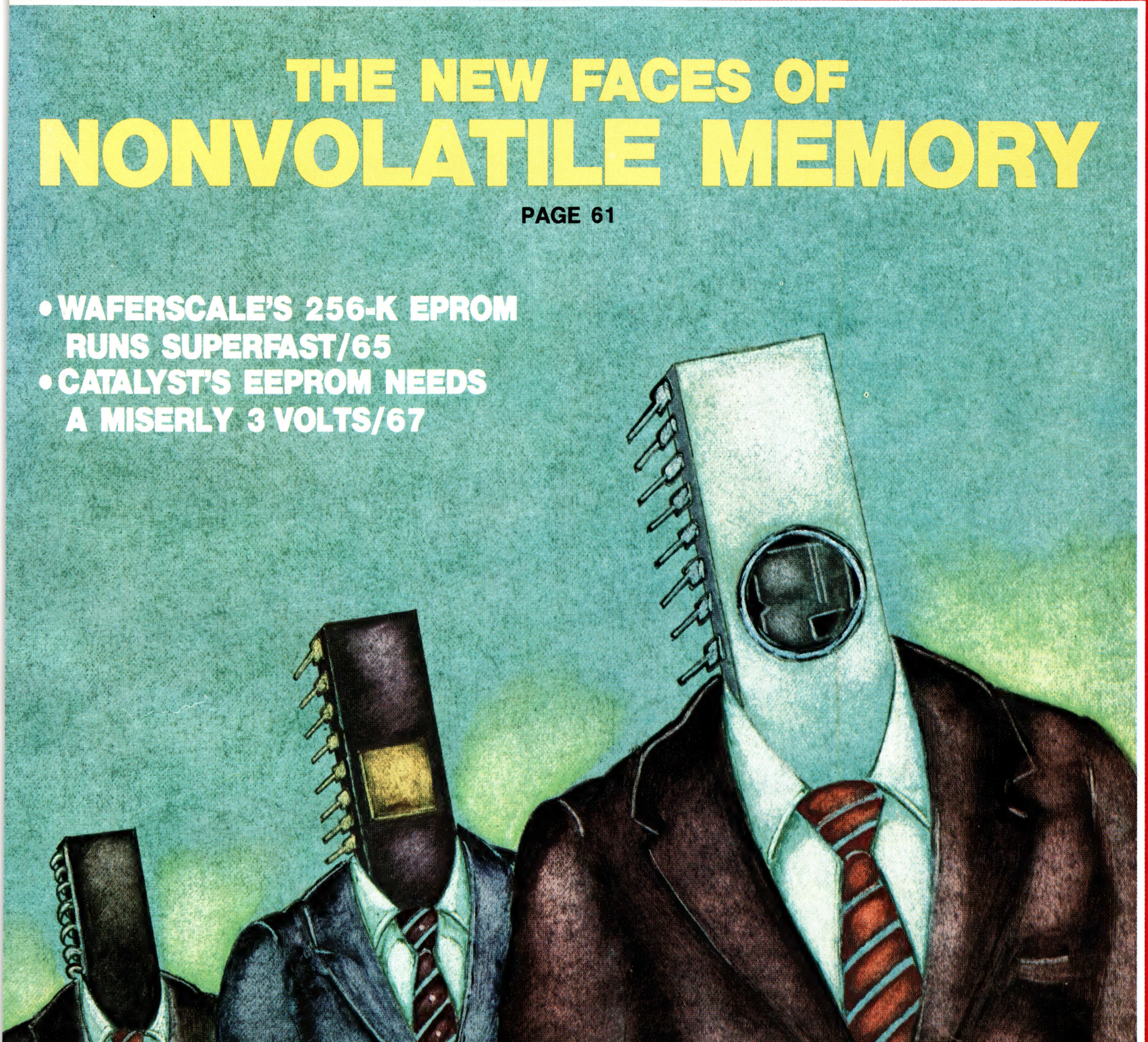

THE NEW FACES OF NONVOLATILE MEMORY

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- CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS/67

Finally, graphics to match your imagination.

INTRODUCING THE FIRST EFFECTIVELY PARTITIONED VLSI ARCHITECTURE FOR TRULY FLEXIBLE GRAPHICS SYSTEMS DESIGN

Imagine a graphics architecture so powerful, you can achieve 16K-by-16K resolution. So effective, you can add virtually unlimited planes of color without degrading performance. So flexible, you can integrate it into an existing design or use it to build an entire range of new systems.

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By using a multiple-chip, modular approach, the Advanced Graphics Chip Set avoids the design compromises and limitations of single chip solutions.

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For more information and availabilities, just contact your local National Semiconductor Sales Engineer or write:

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Circle 1 on reader service card

Electronics

International edition

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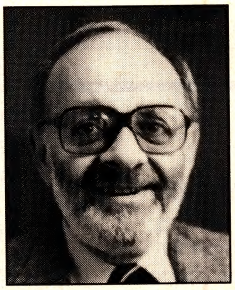
PUBLISHER'S LETTER

It's report-card time again. In this issue we take our annual midyear look at the state of the electronics markets, examining how the growth forecasts for 1987 that are being made now compare with those that were made for our big, first-of-the-year *Electronics* Market Report. The most recent results are on p. 44; the conclusion, in a nutshell, is that in most cases the estimates are being scaled down.

WEBER



WOLFF

Even as we make that comparison, we are using this quick July snapshot as a dry run for our full-blown 1988 U. S. market report, which we will publish in the first issue of 1988. Preparations for that survey—one of our most widely read features—are already under way under the direction of executive editor Sam Weber. Even before most of the people who will contribute to the report have looked into their crystal balls to see what kind of year they and the industry will have next year, Sam is collecting data, revising and fine-tuning the questionnaires that will go to selected companies early in the fourth quarter, and studying various methods of making the survey more valuable to our readers.

"Our basic methodology, which we have perfected over the years since we did our first report in 1958, will be unchanged," says Sam. "For the domestic report, executives of companies that make the equipment or components listed will estimate total U. S. consumption in the markets that they serve. For the overseas reports, the estimate is for consumption in each nation covered. The *Electronics* staff will then analyze the replies, and where necessary supplement the results with more research. We also check with market-research firms to see if their numbers mesh with ours."

For this issue's considerably shorter update, the technique was necessarily altered. Howard Wolff, the associate managing editor who was responsible for editing and producing it, says, "We relied on the reporting of our department and field editors. They questioned their most knowledgeable sources and boiled down the replies."

Wolff continues, "The toughest problem is not getting the information, but reducing it enough to fit in the three pages allotted for the article. For myself, the most difficult obstacles are addition and subtraction. But my family must have heard my complaints, because for Father's Day I got a printing calculator. And I truly appreciated it."

The popularity of our market reports can by judged by the number of letters and phone calls that we get suggesting changes or disagreeing with our conclusions. We don't keep count of them, but typical of the complaints was one letter from a reader who insisted that our calculations were wrong. This alarmed us, so we phoned him and asked how he had decided that. It turned out that *he* had added the figures incorrectly.

So it might be said that the first rule for reading a market forecast is to add the columns correctly. And if that proves difficult, try to borrow Wolff's new calculator.

Laurence Altman

July 9, 1987 Volume 60, Number 14
149,029 copies of this issue printed

Electronics (ISSN 0883-4989). Published biweekly by McGraw-Hill Inc. Publication office: 1221 Avenue of the Americas, N. Y., N. Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P. Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N. Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: MCGRAWHILLNEWYORK.

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- Emulex 14.4-Mbit/s modem will cost the same as 9-Kbit/s units
- Chromatics color display has twice the speed of competitors
- Graphics board more than doubles the resolution of IBM PS/2

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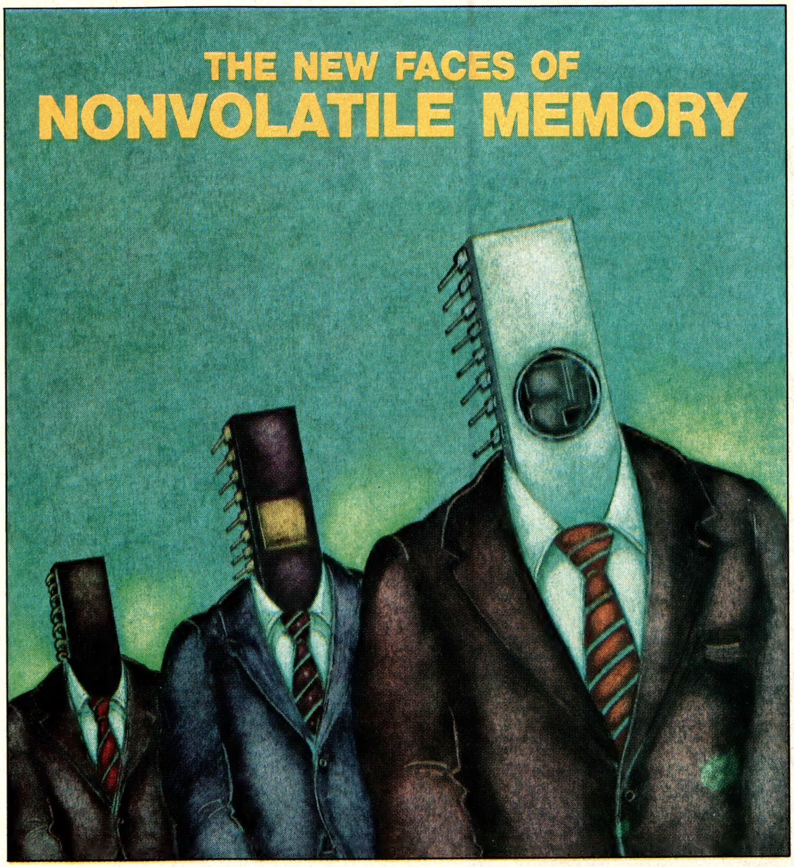
COVER: MICHAEL A. DONATO



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The midyear *Electronics* Market Report is more than an update on our January forecast, it's also a dry run for the 1988 report

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- German firm buys control of CAD pioneer Calay
- Microsoft and 3Com will build OS/2 local network
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- Japan: Sony delays the sale of its 8-mm camcorder
- Japan: Ku-band satellite communications to be tested
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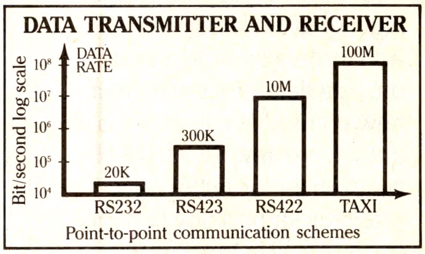
- West Germany: Philips, Siemens in Swiss mobile phone deal

New Products, 52E
- Philips's fast new CMOS logic family joins TI in moving ground and supply pins to center
- A rotary encoder from Canon uses diffracted laser light to achieve 20-arc-sec accuracy
- GaAlAs optocouplers outperform GaAs devices by a factor of five
- Robotechnic's CAD software supports 1,280-by-800-pixel display

Conventional wisdom is fine. For conventional designs.

Imagine a parallel-to-serial converter that lets you move data at 100 Megabits per second. Imagine it working like a register, shooting data into a latch that's stretched from point to point, letting that data race, transparently, ten times faster than conventional wisdom says it can go.

You just imagined TAXI—the Am7968 Transmitter and the Am7969 Receiver—two of the most unconventional, incalculably useful products we've ever offered.



Our new 125MHz analog Phase-Lock-Loop receiver runs ten times faster than the popular 26LS family of RS422 devices. That makes TAXI the highest speed serial data device available. And, where you used to use ribbon cable or bundles, you can design with a single coaxial or fiber optic cable.

Its simplicity and speed don't confine you to a narrow data path, though. Twelve parallel interface pins allow you to operate with data that is 8, 9 or 10 bits wide. TAXI is cascadable, too, in multiples of 8, 9 or 10 bits. They all move through a single cable to get the message across fast.

So now when someone says "You can't move data that way!," you can just smile and say, "Watch."

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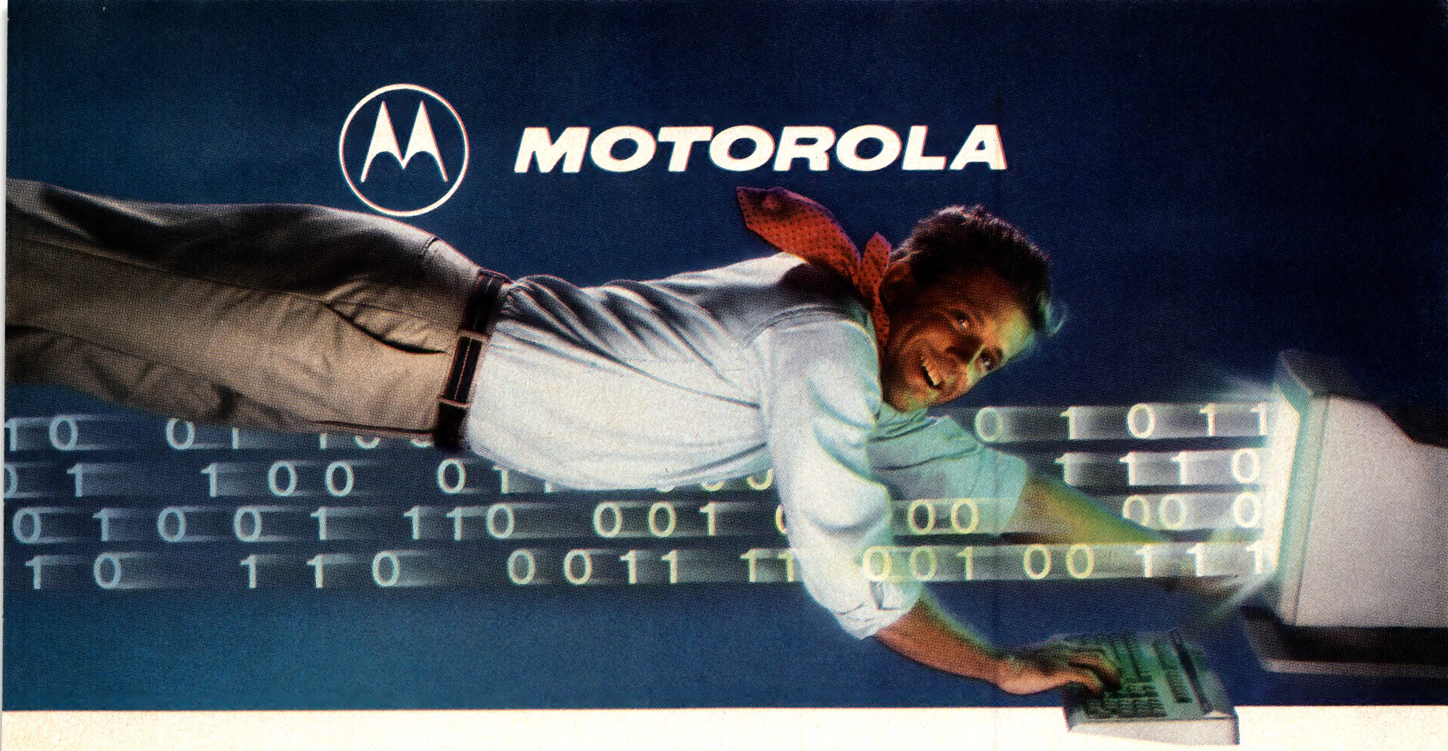


Stick to the truth at top speed.

Keep high-performance memory systems accurate, reliable with F2960/2960A control.

Fact is, today's big, fast memory arrays can separate you from reality with a single data-bit lie. Instantly, without explanation or correction.

Fortunately, there's a way to keep DRAM systems on the straight and narrow: the MC74F2960/2960A EDAC and associated LSI devices.

They do what discrete logic can't: maximize reliability, performance and economy. Without taking up usable board space.

High-speed errata eraser.

The F2960/2960A contains all logic needed to correct any single-bit error and detects all double- and some triple-bit errors. It generates 6 check bits on a 16-bit data field, 7 for 32-bits and 8 for 64 bits according to a modified Hamming code and corrects data in nanoseconds.

Motorola 'A' System Max Speed vs Standard System

Mode	Path	Am2960/61	MC74F2960A/61A	% Improvement
Generate	Total Delay	57 ns	32 ns	44%
Detect	Total Delay	47 ns	29 ns	38%
Correct	Total Delay	100 ns	65 ns	35%

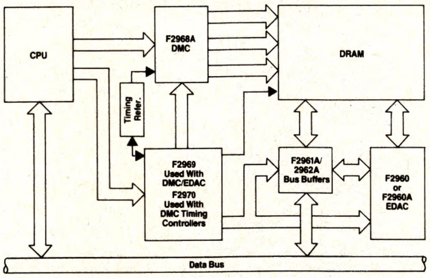
Featuring two diagnostic modes, the cascadable EDAC makes the error syndrome available on separate outputs for data logging.

It's pin-and-function compatible with similar units and utilizes the three-state MC74F2961A/62A inverting/non-inverting bus buffers for multiplexed bus operation.

In a 16-bit system, EDAC and buffers use about half the power of comparables.

What's more, its separate byte controls facilitate byte operations and it's fully compatible with the M68000 or comparable CPU family.

HIGH PERFORMANCE MEMORY WITH F2960A EDAC FAMILY



And support to make it easy.

The controller, MC74F2968A, provides complete address multiplex, refresh and drive for up to 88 DRAMs and interfaces with 16K, 64K or 256K memories.

The MC74F2969 provides all timing signals for memory control with error detection and correction, arbitrates memory cycles, handles refresh timing, memory initialization and supports error logging.

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16K SRAMs		
Device	Process	Access Times
IMS1400M (x1)	NMOS	45, 55, 70ns
IMS1420M (x4)	NMOS	45, 55, 70ns
IMS1403M (x1)*	CMOS	35, 45, 55ns
IMS1423M (x4)	CMOS	35, 45, 55ns

64K CMOS SRAMs	
Device	Access Times
IMS1600M (x1)*	45, 55, 70ns
IMS1620M (x4)*	45, 55, 70ns
IMS1624M (OE, x4)*	45, 55, 70ns
IMS1630M (x8)*	45, 55, 70ns

*Also available as Low Power Battery Backup CMOS SRAMs with Idr of 10µA (typical Icc at 2V at 25° centigrade).

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ELECTRONICS NEWSLETTER

HITACHI'S NEW SUPERCOMPUTER LEAPFROGS CRAY . . .

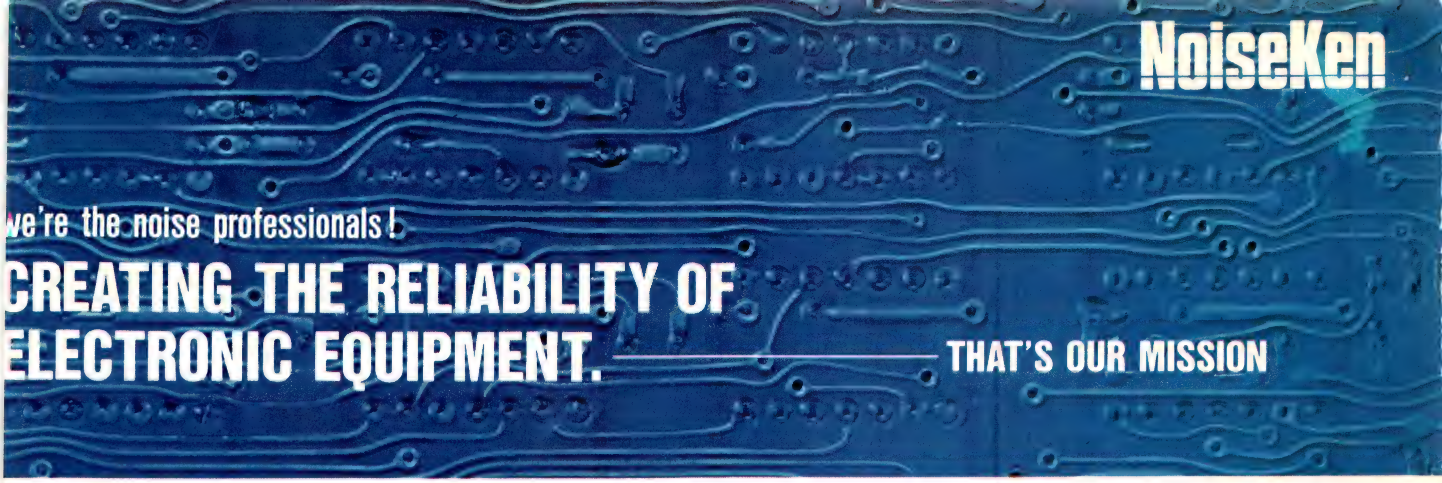
Hitachi Ltd. has unveiled a new supercomputer that can run up to 3 billion floating-point operations/s, putting it smack in the middle of its U. S. competitors. The new S-820 model 80 will compete with several U. S.-made machines, including Cray Research's Cray 2, which runs at about 1.8 gigaflops, and ETA Systems' ETA^{10}, which can do about 6.7 gigaflops. Based on the same chip and assembly technology used in Hitachi's two-year-old M-680H mainframe, the S-820 model 80 gets its added power partly from a 12-pipeline architecture (four more than the M68OH) that lets it operate internally like a multiprocessor machine. Two chips not used in the mainframe and a new memory-extension system also aid performance. The special chips include an emitter-coupled-logic vector register—actually a 7-Kbit random-access memory integrated on a 2,500-gate array that boasts 2.5-ns access times—and Hitachi's own BiCMOS, ECL-compatible, 64-Kbit dynamic RAM, which has an access time of 13 ns, and makes possible a board access time of 20 ns (half that of the M68OH). Main memory capacity for the system is 512 Mbytes, but high-speed file memory can range up to 12 gigabytes. Deliveries will start in the first quarter of 1988, with rental fees beginning at about $545,000 per month. ☐

. . . BUT THE SUPERCOMPUTER LEADER HAS THREE FASTER MODELS COMING

With Hitachi and a myriad of others nipping at its heels, supercomputer leader Cray Research Inc. is not sitting on its hands. The Minneapolis firm is pushing ahead with its plans for three new, increasingly parallel and ever faster supercomputer architectures between now and 1994. First out will be the Y-MP, an eight-processor system based on VLSI silicon technology that is expected to hit a peak speed of 3.2 billion floating-point operations per second. That machine, scheduled for delivery next spring, will be followed by the Cray 3 in 1989 or 1990. Incorporating gallium arsenide chip technology and a 16-processor design, the Cray 3 will up the performance ante to the 12-to-20-gigaflops range. Beyond that, Cray is looking toward the 1992-94 time-frame for production of a system currently code-named the MP. That machine features more processors working in parallel—perhaps as many as 64. Circuit technology for the MP has not yet been determined, but devices based on advanced GaAs high-electron-mobility transistors are a possibility. ☐

A WORRIED TOSHIBA MOVES FAST TO MOLLIFY U. S. AND STOP IMPORT BAN

Look for Toshiba Corp. lobbyists to swarm over Capitol Hill as the Japanese firm strives to appease the U.S. government and thus avoid heavy sanctions for illegally selling high-tech milling equipment to the Soviet Union. The Japanese firm is taking very seriously the strong signal sent out by the U.S. Senate, which on July 1 voted 92-5 to ban Toshiba and its partner in the technology diversion, Norway's Kongsberg Vapenfabrik, from importing goods to the U. S. for at least two years. The day after, Toshiba's top two officials resigned and its U.S. subsidiary hired a Washington law firm to handle its case. Chairman Shoichi Saba and president Sugiichiro Watari said they were taking personal responsibility for the sale, even though they had no knowledge or control over the deal, which was made by a 51%-owned subsidiary, Toshiba Machine Corp. Saba said he would take responsibility "for not creating an atmosphere throughout the Toshiba group that would make such activity unthinkable." Toshiba Machine sold $23 million worth of equipment for manufacturing submarine propeller blades to the Soviets in 1983 and 1984 [*Electronics*, June 11, 1987, p. 53]. The Senate action, part of a broader trade bill, is not final; although the House is considering similar legislation, the Reagan administration is opposed to the general bill. ☐



we're the noise professionals!

CREATING THE RELIABILITY OF ELECTRONIC EQUIPMENT.

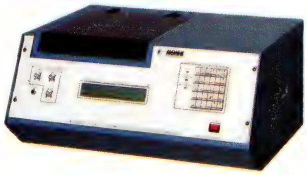
THAT'S OUR MISSION

ELECTROSTATIC DISCHARGE SIMULATOR

A testing machine designed to simulate electrostatic discharge which may occur between a charged body such as human body and electronic equipment.

ELECTROSTATIC DISCHARGE SIMULATOR FOR SEMICONDUCTORS

Automatic test equipment designed to simulate the electrostatic discharge which may occur between a charged body and a semiconductor. Presetting the voltage to be applied, the number of pulses, and the pins to which the voltage will be applied allows testing to be carried out with a high degree of accuracy.

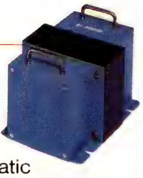


ESS-910G

LIGHTNING SURGE SIMULATOR

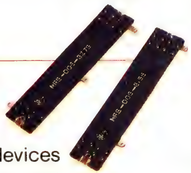
Test equipment designed to simulate lightning surges which may damage low voltage control circuitry. This equipment facilitates surge testing (such as FCC Part 68, paragraph 68-310) by superimposing a transient signal directly onto the power supply line.

NOISE CANCELER TRANSFORMER



A transformer designed to protect against impulse, lightning surge, and electrostatic discharge.

NOISE CANCELER



Devices used to reduce noise on printed circuit boards. These devices can be mounted on printed circuit boards in the same manner as integrated circuits, or mounted on loaded printed circuit boards as an additional element.

POWER LINE DISTURBANCE DETECTOR

Connected to the power supply line, NDR-544 monitors supply voltage fluctuations (simultaneously on AC line and DC line), frequency variations, and impulse noise.

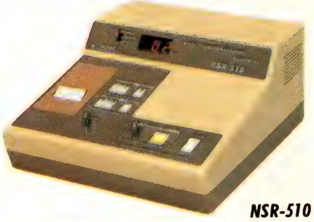
IMPULSE NOISE SIMULATOR

Test equipment designed to determine electronic equipment tolerance to transient signals which may superimpose on the power supply lines.

NOISE COUNTERMEASURING EQUIPMENT

This model is provided to take proper noise preventive measures for P.C.Bs loaded with CPU, I/O and RAM.

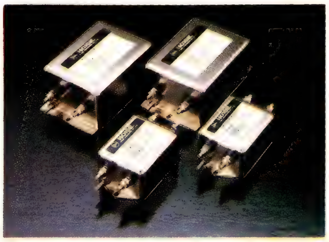
It consists of impulse noise generator, electric potential measuring unit and counter plane.



NSR-510

VOLTAGE DIP SIMULATOR

Test equipment designed to simulate a momentary voltage drop or the momentary power failure which may occur on a commercial power supply line and adversely affect sensitive electronic equipment.



IMPULSE NOISE FILTER

A high performance filter to suppress power-line noise which may adversely affect the operation of electronic equipment. These filters also prevent noise produced by the equipment from superimposing signals on the power supply line.

In addition to the above-mentioned,
please contact a Noise Laboratory's Sales Engineer to discuss your specific requirements.

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Circle 23 on reader service card

PRODUCTS NEWSLETTER

MIPS RISC PROCESSOR IS TWICE AS FAST AS 80386 YET COSTS NO MORE

Work-station manufacturers can now buy a reduced-instruction-set processor from MIPS Computer Systems Inc. that delivers twice the performance of Intel Corp.'s 80386 microprocessor for about the same price. Available in 12.5- and 16.67-MHz versions, the R2000 chip's RISC architecture provides enough processing power to drive work stations at a pace of between 8 million and 12 million instructions/s, depending on clock speed, cache memory, and other system-design variables—compared with 4 to 5 mips for 80386-based work stations, says the Sunnyvale, Calif., company. The 12.5-MHz version will sell for $195 in 5,000-unit quantities; the 16.67-MHz version, $295. Both are available now. Systems software and third-party tools are also available for another $100 per CPU. ☐

EMULEX 14.4-KBIT/S MODEM TO COST THE SAME AS 9.6-KBIT/S PRODUCTS

Look for computer-products specialist Emulex Corp. to break into the communications hardware market with a 14.4-Kbit/s modem that offers a 50% performance advantage over the 9.6-Kbit/s modems now standard for leased-line transmissions. A proprietary CMOS six-chip set is the key factor bringing the Performance 1000 full-duplex modem in at just $1,795—about the same price as the 9.6-Kbit/s modems, claims the Costa Mesa, Calif., company. The chip set also delivers a 50% reduction in component count, which contributes to an 8½-by-11-in. footprint for the 2½-in.-high modem—the smallest available at 14.4 Kbits/s. The modem also features menu-driven operation monitored by a liquid-crystal display. Available now, the modem conforms to the CCITT V.33 standard. A 9.6-Kbit/s version conforming to the V.29 standard sells for $1,295. ☐

CHROMATICS COLOR DISPLAY HAS DOUBLE THE SPEED OF COMPETITORS

By implementing the industry-standard Graphical Kernel System software in microcode, Chromatics Inc. has come up with a color display system that draws 1 million fully transformed two-dimensional vectors per second—double the speed of competitive systems. The LeMans Colorgraphic Display can also draw 250,000 three-dimensional vectors/s and generate 25,000 smooth-shaded polygons/s with hidden-surface removal in 3-d applications. Its graphics engine is based on multiple processors arrayed in a 32-bit pipelined architecture. A standard 32-bit VMEbus interconnection provides an open architecture that interfaces easily with host computers from Sun Microsystems Inc. or Digital Equipment Corp.'s VAX series. Available in the third quarter with a 1,280-by-1,024-pixel display, the LeMans costs $25,000 each; volume discounts are available. ☐

GRAPHICS BOARD MORE THAN DOUBLES RESOLUTION OF IBM PS/2

A color-graphics controller board from Control Systems Inc. boosts the standard 640-by-480-pixel resolution on IBM Corp.'s Personal System/2 products by factor of more than 2.5—to a resolution of 1,024 by 768 pixels noninterlaced or 1,024 by 1,024 interlaced—while at the same time maintaining compatibility with IBM's video-graphics-array standard. Built around Hitachi Ltd.'s ACRTC graphics processor, the Artist 10/16 VGA board also offers a 16-color palette and 1 Mbyte of on-board graphics memory. A redesigned version of the company's Artist 10/16 for IBM's Personal Computer family, the new controller board plugs into a 136-connector slot in the PS/2 motherboard to work effortlessly with the machine's Micro Channel architecture. The Artist 10/16 VGA will be available in August from the St. Paul, Minn., company for $1,797 in 100-unit quantities. ☐

If it happens in a blink, we'll catch it.

Analog Solutions' 10-bit, 25 MHz A/D converters capture every event in a fast-changing analog world.

Some companies only deliver components. We provide complete solutions.

Our latest is the ZAD1025, a vastly improved Video ADC offering the features that system designers have been asking for.

The ZAD1025 delivers true 10-bit performance at a 25 MHz sampling rate. So if you're doing video digitizing at speeds below 25 MHz, you don't have to pay extra for a super fast 40 MHz converter.

Furthermore, if you're designing test or imaging systems, why be limited to a single optimal sampling rate? Our ZAD1025 offers variable sampling rates from DC to 25 MHz with 10-bit linearity over the entire range.

The ZAD1025 uses 40% less power than any other design on the market–only 13 watts. Add to that our custom LSI which reduces the overall parts count, and you have inherently better reliability.

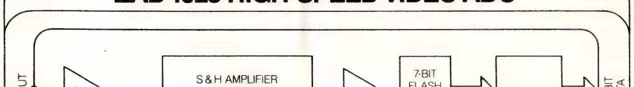
Finally, our 1025 is pin compatible with the industry standard MOD1020.

All this may suggest you'll be paying more than you would for a typical 20 MHz converter.

Well, you won't. We're competitively priced. Which may inspire you to reach for the phone at something approaching the speed of light.

The ZAD1025 is the first product in Analog Solutions' new family of video converters. For more information contact Analog Solutions, 85 W. Tasman Drive, San Jose, CA 95134-1703, (408) 433-1900, FAX: (408) 433-9308.

ZAD 1025 HIGH-SPEED VIDEO ADC



FUNCTIONAL BLOCK DIAGRAM

• 10-bit resolution • 25 million samples/sec. • 0.1% accuracy
• Superior linearity • 5" X 7" open board construction

ANALOG SOLUTIONS

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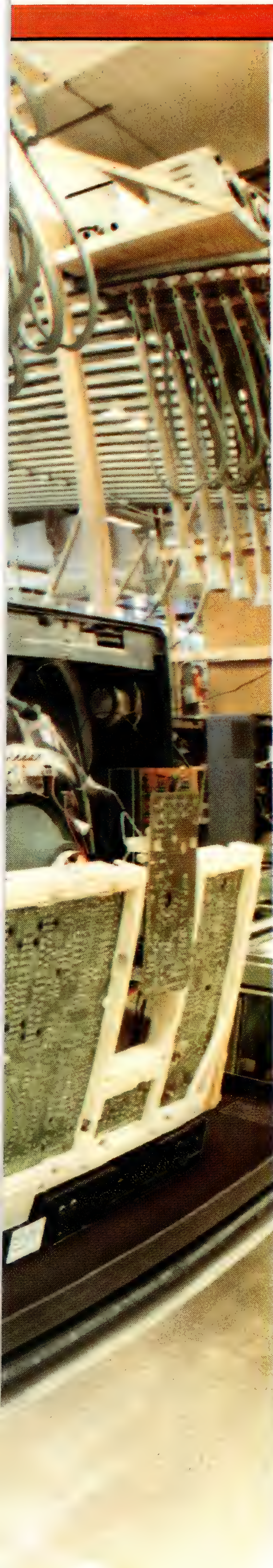
Circle 27 on reader service card

PHILIPS

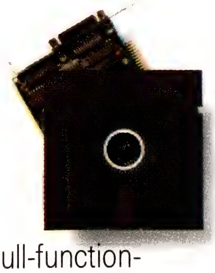
functional board testing:

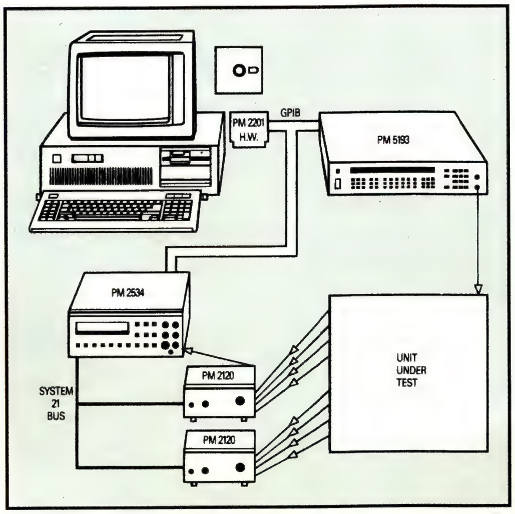


Problem. Volume production of a new TV receiver called for full-performance testing of tuner functional boards.

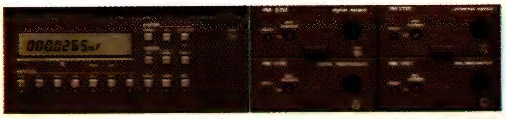
Analysis. A major TV manufacturer, demanded a fast, accurate, reliable and easy to apply testing procedure on every board. Moreover, the test system had to be highly flexible and simple to expand to allow for future changes both in the unit-under-test and rate of production.

Action. By means of a software-controlled interface card **PM 2201**, the customer's own PC was converted into a powerful GPIB controller, while a **PM 5193** 50 MHz full-function-generator, connected between the GPIB output of the PC and the customer-designed test jig, provides up to 8 selectable waveforms and a choice of modulation modes.





Clear, precise readout of test results is by means of a **PM 2534** digital multimeter and the PC monitor. A high level of system flexibility is assured by connecting universal switch modules of Philips **System 21** between the DMM and the unit under test.



Conclusion. GO/NO-GO test procedures are simple, fast, precise and, above all, extremely economic. Equally important, the test system can easily be re-set and reconfigured to meet new performance and/or production requirements as and when the customer wishes.

One of the world's largest electronics companies, Philips is both a major manufacturer and user of an extremely broad range of test and measurement instrumentation. Thus we are uniquely qualified to develop cost-effective solutions that meet your system needs, perfectly.

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CAE IS FINALLY BEGINNING TO LIVE UP TO ITS PROMISE

FASTER PLATFORMS AND SIMULATION PACKAGES PROVIDE THE IMPETUS

MIAMI BEACH

In the annals of computer-assisted engineering, 1987 could well go down as the year the pieces came together. For the 107 exhibitors and some 4,000 showgoers at the Design Automation Conference in Miami Beach, the five-year-old promise of CAE—to speed product development even as it leads to better products—began to come true.

The big trends are clear. In hardware, it's faster and far less expensive workstation platforms; in software, it's more sophisticated simulation along with improved simulation models.

With the parade of work stations taking on the character of a mips war, Apollo Computer Inc. took the conference spotlight by unveiling its Domain series 4000 Personal Super Workstation (see p. 32). The machine, rated at 4 million instructions per second, can do simulation of 100,000 gates, complete system timing, and testability analysis—a run that previously required an accelerator.

The series 4000, at under $19,000, is today's price-performance leader, but the field is jammed. Digital Equipment Corp. has jumped in with its new $7,900 color VAXstation line [*Electronics,* June 25, 1987, p. 42]. Intergraph Corp. has a new under-$30,000 5-mips model, and Sun Microsystems Inc. is joining the bunch with a 10-mips machine. Hewlett-Packard Co.'s new $69,000 Model 825SRX carries 8-mips credentials.

Hand in glove with more powerful and cheaper platforms are faster simulators. For example, Cadnetix Corp. of Boulder, Colo., introduced its Configurable Analysis Engine, a network processing node that accelerates the compilation of data required for a simulation run even as it performs the digital and analog simulation process itself.

Another new class of simulators runs as fast as those requiring high-performance hardware—but without the hardware. Typical is the Verilog simulator from Gateway Design Automation Corp. of Westford, Mass. "In addition to full behavioral language, Verilog-XL simulates at the gate and even switch levels, and works faster on a work station than most hardware accelerators costing $100,000," says Prabhu Goel, president.

Simulators are being improved in other ways, too. LSI Logic Inc. of San Jose, Calif., unveiled a revamped LSIM, the first multimode simulator, which offers behavioral, logic, switch, circuit, analog, and fault simulation. The new version also has an interactive waveform viewer that lets designers pan and zoom and make voltage and timing measurement directly off the waveform. Through multiple simulation windows, the designer can view simultaneous inputs and outputs in both alphanumeric and waveform displays, says Van Lewing, director of software marketing.

While some suppliers are adding functions to their simulators, others are tailoring their products to run on lower-priced work stations. One such product is from Orcad Systems Corp. of Hillsboro, Ore. The company says its new simulator can easily handle designs with as many as 14,000 gates on a standard personal computer with an extended graphics card and 640 Kbytes of memory.

But simulators are no better than the models they run. "A simulation engine without good models is like a car without wheels," says Richard Perry, marketing vice president of FutureNet, a division of Data I/O Corp. in Chatsworth, Calif. "There aren't enough models out there, especially ones certified by the IC vendor." To address this problem, Logic Automation Inc. of Beaverton, Ore., and Quadtree of Bridgewater, N. J., have embarked on ambitious programs to have their models certified by IC vendors.

–Jonah McLeod and Stan Runyon

AUTOMATED SOFTWARE DESIGN IS TAKING OFF, TOO

Computer-aided software engineering is fast becoming a critical component in an increasing number of electronic design automation systems. Many of the EDA system vendors at the Design Automation Conference in Miami Beach are adding CASE to their product lines. Digital Equipment Corp., for example, announced a cooperative marketing program with Cadre Technologies Inc. to include its Teamwork series of CASE tools in DEC's stable of EDA applications. DEC also has a marketing agreement with Tektronix Inc. for its CASE tool set. Hewlett-Packard Co. is also offering Teamwork.

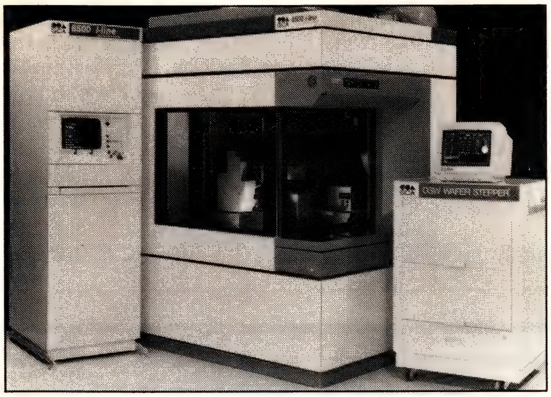
CASE products promise faster software development with fewer errors. The coupling of computer-aided documentation to CASE adds another measure of productivity and control. Vendors are working to tie both types of tools intimately into their EDA systems.

At Miami Beach, Cadre Technologies, one of the leading vendors of CASE tools, proposed a standard for interfacing CASE to existing EDA applications. Cadre has suggested an extension to the EDIF—Electronic Design Interchange Format—standard for interchanging data among CASE tools and other EDA applications.

Context Corp., a Mentor Graphics Corp. subsidiary that markets a computerized documentation system, maintains that automated documentation tools will play a critical role with CASE in integrated EDA systems. Context's system goes beyond computerized document preparation and publishing. It manages and controls all hardware and software changes to system-design documentation. Context's change-control feature can become the basic tool in an EDA system for management of a product development project.

As with the other functions in an EDA system, CASE and documentation tools must be tightly integrated to be most effective. An example of integrating CASE and computerized documentation is the system the Boeing Co. put together for itself. The Boeing Automated Software Engineering system includes a system design environment from Teledyne-Brown, a structured analysis software development environment from Cadre, and the Context documentation system, all using the same data base.

–Tom Manuel



WINNER. Beleaguered GCA considers an $8 million order for DSW 8500 steppers a sign that the worst might be over.

ile, and will continue to be so until conditions in our industry improve."

GCA makes other equipment, but steppers determine its fortunes. They account for half the company's revenues and are the primary tool pitted against X-ray lithography in the battle to reach integrated-circuit line dimensions of 0.5 μm and less. The main competitor for GCA, which has a 35% market share worldwide, is Japan's Nikon Precision Inc., whose share is believed to be about 25%.

However, Rick Ruddell of Rudell & Associates, a Redding, Calif., market researcher who follows the stepper business closely, says that ASM Lithography, Tempe, Ariz., is coming on strong in the market. Ruddell also maintains that while GCA can win some short-term gains, the company's future "lies in being acquired. Potential buyers see [GCA's] installed base as an entrée into a global market."

GCA's comeback started under Richard Rifenburgh. Rifenburgh, a specialist in company turnarounds, was brought in as chairman, president, and chief executive officer in March 1986 to salvage GCA. He quickly set in motion the steps that preceded a financial-restructuring plan that was implemented this spring. The company shed three divisions, consolidated operations, and laid off 1,280 employees—cutting its payroll to 1,000.

At the same time, Simone, then a senior vice president (he succeeded Rifenburgh as president in February), and other members of senior management were laying the technology base to enable the company to benefit from its own recovery, and from any rebound in the market. "We set and achieved several goals, even though we were running out of cash. It's amazing what you can accomplish when your pants are on fire," Simone says.

GCA isn't out of the woods yet. The company's first quarter ended with revenues of $13 million and a $12 million loss, which Simone says resulted from customers' postponing orders until the restructuring plan was approved in March. He's buoyed, however, by continuing increases in semiconductor book-to-bill ratios, and by the fact that U. S. semiconductor manufacturers do not have much photolithography equipment that can produce lines finer than 1.5 μm.

GCA has developed a lens system for an excimer laser source for its steppers, to deliver the shorter wavelengths required for 0.5 μm. Simone believes that will keep optical lithography competing against X-rays. *–Larry Curran*

SOFTWARE

PLUG-IN SOFTWARE MAY SAVE BIG BUCKS

HIGHLAND HEIGHTS, OHIO

Computer hardware users take for granted the ability to tailor a system by mixing and matching boards that simply plug into a machine's backplane. Now Allen-Bradley Co. is out to match that flexibility in software.

With its eye on the factory-automation business, the company plans this summer to ship the first modules based on an ambitious new software scheme called the Software Backplane. Under development for three years, it is billed as a generic approach to factory-cell-control software: it will allow systems integrators to develop application packages as standard, portable modules that can be plugged in and played on the plant floor regardless of the host operating system employed.

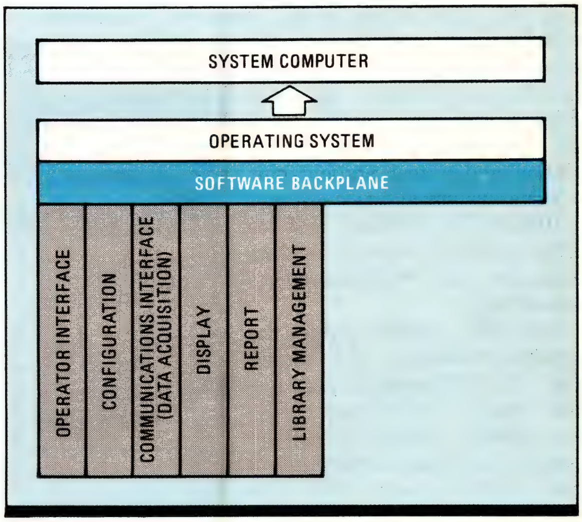
HALF THE COST. Because separate application packages won't be required for differing host systems, the approach could eventually halve the software-development costs of complex custom factory-automation systems, says Richard L. Eshleman, director of marketing at Allen-Bradley's Industrial Automation Systems Division in Highland Heights, Ohio. What's more, it could cut by 90% the cost of building systems based on a set of standard application modules, while also boosting software reliability and maintainability, he adds. The concept will be tested at "a large automotive customer site" starting this summer, and will be offered as a standard product next year, Eshleman says.

"For the high end of the cell-control business, the Software Backplane is our answer," declares J. Tracy O'Rourke, president and chief executive officer. The concept is a major piece of the firm's strategy to maintain a leading position in the cell-control business. That market is expected to grow by some 40% annually to total $1 billion worldwide by 1990.

As the name implies, the Software Backplane architecture is modeled after that of a hardware backplane. A hardware backplane combines a standard physical interconnect for the transfer of data with a protocol to manage those transfers; the Software Backplane is a software layer that provides a logical interconnect and a protocol for linking application modules to a specific computer operating system. The initial version will be for Digital Equipment Corp.'s VMS operating system.

Though yet to be proven, the concept is already drawing raves from some observers. "The potential for this is tremendous," says Daniel R. Kosmalski, division manager for Merit Systems Inc., a Troy, Mich., factory-software developer. Other vendors offer software tools designed to help isolate application software from changes and constraints in the host-system architecture, Kosmalski allows, but these tools are tied to specific hardware or operating systems.

"There are all sorts of different communication protocols like MAP [Manufacturing Automation Protocol] and Eth-



SOFTWARE BACKPLANE. With the Software Backplane, users will be able to plug in standard, portable applications packages.

It's an
issue that
will be talked
about for
the entire
year...

The August 6th issue of Electronics

An entire special issue that sets the record straight on ASICs.

There's been a lot of talk lately about the changing roles of traditional IC makers and their custom and semicustom IC counterparts. And everybody seems to have a different opinion.

In a comprehensive special report in the August 6th issue of *Electronics* magazine, our editors do some tough reporting on the subject. Discussing the current and future status of commodity IC producers and ASIC houses. What new technologies they're developing. What changes we can expect to see in their marketing strategies. And what it all means to semiconductor specifiers.

If you're a semiconductor manufacturer—whether a commodity IC maker or a producer of custom ICs, semicustom ICs, gate arrays or standard cells—don't miss being a part of this important special issue. More than 131,000 decision-making technical managers and senior engineers won't be missing a word of it.

Here are some of the hot issues our editors will be reporting on.

- **What the traditional IC makers are up to in ASICs.**
  The newest technologies, processes, and manufacturing techniques from the U.S., Japan, and Europe.
- **How semicustom IC houses are retaliating.**
  New strategies and new design tools they're using to keep competitive. Is better customer service alone sufficient? Will they soon be offering their own standard parts? Must they merge to compete?
- **Profiles of the major players.**
  An examination of the tactics and strategies of both the large commodity IC manufacturers and the smaller niche companies.
- **What's new in related ASIC topics.**
  Coverage of ASIC testing, CAE tools, programmable logic devices, and users' views.

Ten *Electronics* editors from around the world will contribute their insight and worldwide perspective to this special issue.

From San Mateo: Bernie Cole, George Sideris, Jonah McLeod

From Los Angeles: Larry Waller

From Dallas: Rob Lineback

From New York: Stan Runyon, Jeremy Young

From London: Steve Rogerson

From Frankfurt: John Gosch

From Japan: Charlie Cohen

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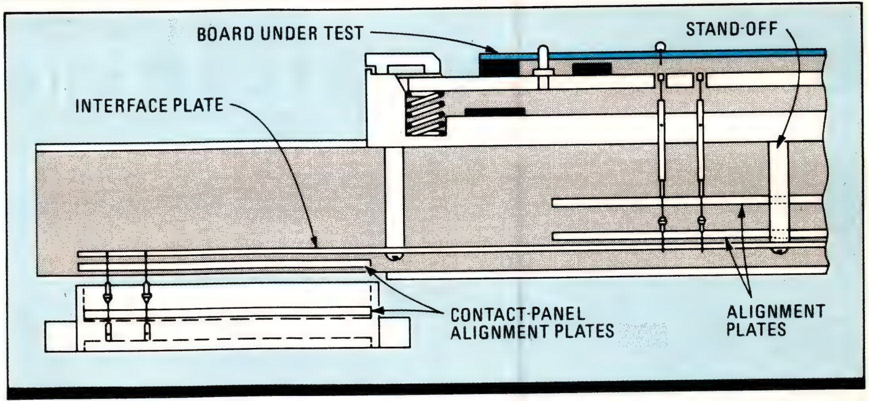
McGraw-Hill Electronics

wire is used or where the wires will go. In addition, with a Multiwire interface board it is possible to have a board with a controlled or matched impedance. This will mean fewer propagation delays within the fixture as well as low cross-coupling.

There are other advantages to be gained as a result of the repeatability feature. For one thing, the printed circuit to be tested and the pc board to be used as a test fixture can be designed at the same time. For another, the use of pc techniques promises a faster process: one week rather than the three to four weeks needed to turn around conventional fixture interfaces. Finally, better control of the process means fewer wiring errors and simpler troubleshooting.

The setup is uncomplicated. On both the board types, push-on connectors soldered to the board mate with the test-contact panel posts. Printed-circuit conductors or multiwired connections run from these points across the board to a matrix of pins at the other end. The pins, in turn, are pushed onto connectors in a contact block.



ELIMINATING THE WIRES. Factron/Schlumberger's Thinline test fixture does without the tangle of wires that links test probes in today's fixtures to the tester's output connector.

Factron is evaluating pc-board versions of its wireless fixture and has multiwired versions on order. Tests to compare performance of the old and the new will start shortly. As for price, Factron figures that even though pc boards and Multiwire are more difficult to make than bed-of-nails fixtures, it can charge close to what the old ones cost because of economies of scale in manufacturing. *–Jerry Lyman*

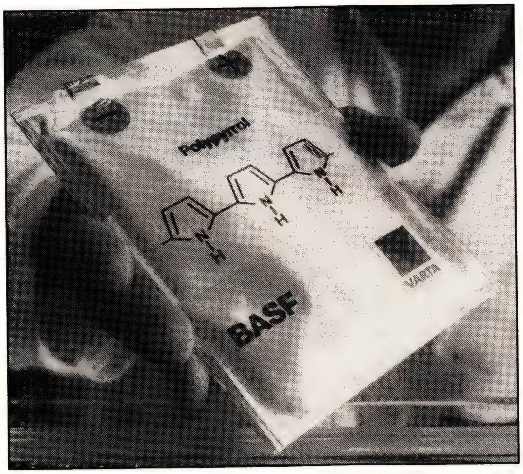
POWER SOURCES

THIN PLASTIC BATTERY BENDS TO FIT

KELKHEIM, WEST GERMANY

If two West German companies are right, the layout and design of portable electronic equipment will start to change radically in the early 1990s. That is when these companies expect their flexible plastic battery to become a viable product.

The two are developing the battery together. Varta Batterie AG is contributing its know-how in battery engineering, and BASF AG is lending its expertise in polymers. Designers will be able to gain space as well as freedom in arranging components by installing the postcard-size cells flat at the bottom of equipment. Or, since the cells can be bent just like cardboard, they can be formed to the contours of the equipment.



WRAPAROUND. The 4-mm-thick polymer cell puts out 3.6 V. It can be installed flat or wrapped around components.

Varta, Europe's leading battery maker with $1 billion in sales last year, is discussing the final shapes of the polymer cells and their application with equipment makers, says Reinhard Gereth, who is responsible for research, development, and technical operations at Varta's research laboratories in Kelkheim, near Frankfurt.

The Varta-BASF cell uses polypyrrole for the positive electrode and lithium for the negative. The polypyrrole is a 50-μm-thick foil and the lithium 100 μm. In addition, an organic electrolyte, typically propylene carbonate with lithium perchlorate as the solute, is used.

The cell puts out 3.6 V under an open circuit and from 3.6 V down to 2 V under load conditions. The present laboratory versions come in two forms: with the electrode foils rolled into a tight cylinder the same size and shape as the familiar AA battery (50 mm long and 14.2 mm in diameter), or as a flat aluminum-covered sandwich 4 mm thick, about the size of a postcard and almost as flexible.

An electrical advantage is the cell's higher output compared with today's nickel-cadmium types, which put out only 1.2 V each. This means more voltage with fewer plastic cells. Also, at 20 to 30 Wh/kg, the gravimetric energy density of the Varta-BASF cell already matches that of the established NiCad type. And at its present state of development, the new cell can go through about 500 successive charge/discharge cycles, each at a 100% depth of discharge from the maximum 3.6-V value to the minimum 2-V level.

Those values, after five years of work by Varta and BASF, lead Gereth to say: "We believe [we are] ahead of other companies working in the field," which includes Allied Corp. of the U. S., cooperating with Hitachi Ltd. of Japan, as well as Japanese car maker Toyota.

Nevertheless, he concedes that the figures are not high enough for a good commercial battery. For one thing, the energy density must be at least doubled; for another, the number of charge/discharge cycles must be raised to at least 1,000. Both can be achieved during the next few years, Gereth says.

The idea of the polymer battery dates back to 1977, when Alan G. MacDiarmid, a professor at the University of Pennsylvania, found that nonconducting plastic materials having conjugated double-bonding of carbon atoms can be made to conduct by electrochemical oxidation or reduction. The early U. S. researchers used polyacetylene as the active material, which proved to be chemically unstable.

At Varta and BASF, investigation of conducting plastics eventually led to polypyrrole, which is stable both in the air and in many organic electrolytes. This property, plus the fact that polypyrrole can be made in foil form, allows the development of an easily producible polymer cell. *–John Gosch*

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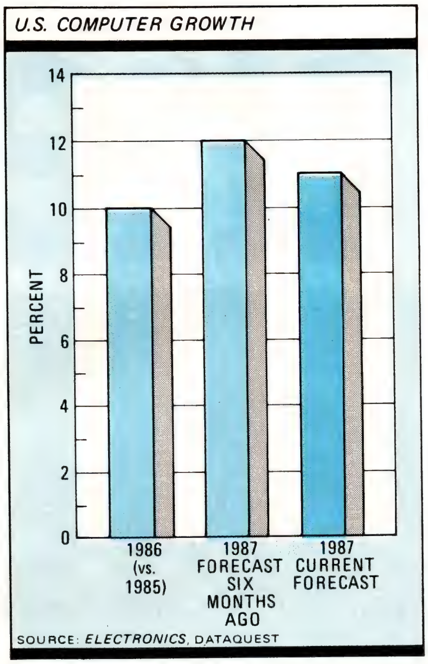

U.S. COMPUTER GROWTH

SOURCE: *ELECTRONICS*, DATAQUEST

up from some $71 billion last year.

Most industry executives are finding more positive than negative signs amid general economic conditions that include increased capital spending, a dollar decline that should stimulate computer purchases in the manufacturing industries, and continued low inflation.

Of course, compared to the 20% growth rates of the late 1970s and early 1980s, 11% to 12% is anemic, and some executives are still more cautious than optimistic. The leading optimists are executives at companies positioned to exceed the industry's overall growth. One of those companies, Digital Equipment Corp. of Maynard, Mass., showed revenues up a rousing 25% to $2.4 billion in its most recent quarter. However, DEC's chief economist, James B. Whittaker, is holding to his original forecast for the industry: up 7% to 10% for the year.

The technical work-station and personal-computer segments appear to be coming back strongly. Apollo Computer Inc., the Chelmsford, Mass., provider of networked work stations, reported a robust first quarter. Revenues were up 50% from the same period last year, to $123.4 million.

At Compaq Computer Corp. in Houston, 1987 is shaping up as an excellent year. It's been so good to date, says Mike Swavely, vice president of sales and marketing, that Compaq has revised upward the forecast for the market segment the company serves—business computers sold through distributors and dealers—to 20% to 25% from the 15%-to-20% range.

The biggest player, IBM Corp., said at the end of June that it has shipped more than a quarter million units of the Personal System/2 line, which was introduced in April. It also expects its personal computer division to post record earnings for the year.

Joining the believers that a recovery is under way is James Bloom, executive vice president for marketing, planning, and operations at Honeywell Bull Inc., the company that emerged from the joining of the computer operations of Honeywell, NEC, and Groupe Bull. Bloom, who is located in Phoenix, says, "I have to feel that we're seeing a gradual but steady turnaround."

However, one tracker who isn't ready to subscribe to the turnaround theory yet is Gerald Kokos, executive assistant to the president and director of investor relations at Prime Computer Inc., Natick, Mass. He says his company met its first quarter plan, which resulted in a revenue increase of 13% over 1986 to $221.7 million. And while he says the second quarter is also on plan it isn't coming from market growth.

"While some prophets are saying we're in the midst of an upturn, we don't see that," he says. "We went into the year with a forecast that assumed 1987 would be similar to 1986, with no big upturn. We're saying we'll see more of the same in the second half" because of anemic capital-spending growth.

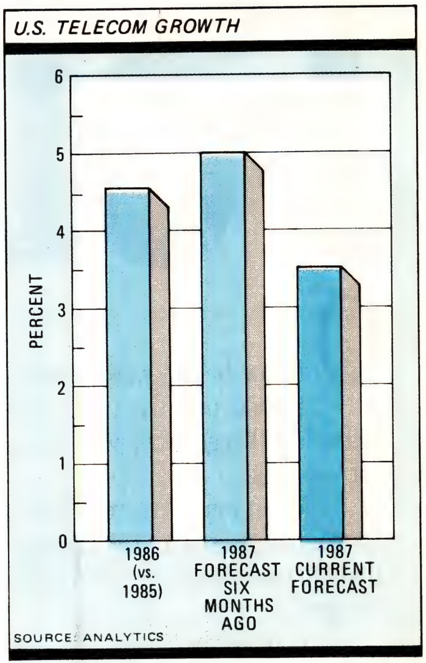
Industry standards and advanced technologies are fueling growth for the Technical Computer Operation at Hewlett-Packard Co., Cupertino, Calif. But Carl Flock, marketing manager there, isn't ready to jump on the turnaround bandwagon yet, either. "The industry has been doing a lot better, and while our situation has been good, I don't want to read too much into our experience."

COMMUNICATIONS

The picture for the U.S. telecommunications industry seems to be worsening. This year "is probably going to be the lowest-growth year for the communications industry" in the current five-year cycle, says Kent Webb, vice president of research at Analytics, a Palo Alto, Calif., market researcher.

Things were better in 1985 and '86, and they'll be better in 1988 and '89, he says. But for now, "we've reached bottom." Analytics has reduced its forecast of 1987 growth to 3.3% from the 5% it predicted in January, compared with the 7% foreseen by companies surveyed for the *Electronics* January 1987 Market Report.

The biggest damper for 1987 so far has been a disastrous first quarter, in which orders tumbled 11% to $16.837 billion, compared with the fourth quarter of 1986 when $18.943 billion in communications equipment was ordered in the U.S. That's unusual, Webb says, because orders usually pick up in the first quarter. "We pulled them [the yearly figures] down because the first quarter pulled them down," he says.


U.S. TELECOM GROWTH

SOURCE: ANALYTICS

The big disappointment so far has been the lack of impact of the integrated services digital network. "ISDN certainly doesn't seem to have had any impact on total market growth yet," Webb says. That's despite AT&T Corp.'s assertion that "we continue to view 1987 as the year of ISDN."

Generally, there is a feeling of stagnation. "We are seeing a lot of indecision, and a lot of people are delaying [purchases] for various reasons," says Janet Boling, manager of strategic planning at Intecom Inc., a wholly owned subsidiary of Wang Laboratories Inc. based in Allen, Texas.

One insider in the PBX industry says times are hard and don't seem to be getting better. The PBX market, he says, has been nearly flat compared with 1986—and that figure was down from 1985. "There might be slight growth, but I think it will end up being pretty flat."

But all signs are not bad. Webb says inventories are shrinking, which is good news for equipment makers, who only recently started to really move their wares. So 1988 looks better, with growth hitting 8%. In fact, Dataquest predicts compound annual growth averaging 8.2% through 1992.

TEST & MEASUREMENT

Unless the market picks up substantially in the second half of this year, test and measurement sales in the U.S. may not even gain the low 3% growth, to $6.5 billion, now forecast for 1987. And this forecast is only half the

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MENTOR GRAPHICS PULLS AWAY IN ELECTRONICS CAD/CAE RACE

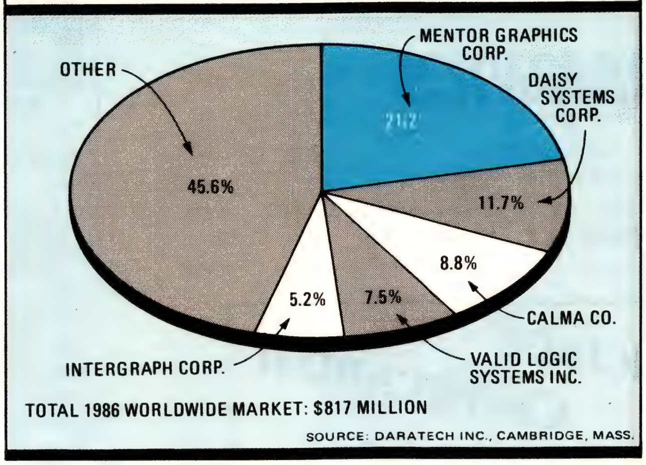
IT CLAIMS A MARKET SHARE LARGER THAN DAISY, TEK, AND VALID COMBINED

by Tom Manuel

The sweet smell of success permeates a group of buildings in a corner of Beaverton, Ore., where the people from Mentor Graphics Corp. hang out. The company is now clearly No. 1 in the new electronic design-automation industry, an industry it helped to create. Starting in 1981, the fledgling company produced an integrated system of applications for electronic design automation on a network of powerful work stations.

During the developing years of that market segment three major competitors emerged, battling for leadership—Daisy Systems, Mentor, and Valid Logic Systems. From 1983 to the end of 1985, Mentor and Daisy Systems Corp., running neck and neck, moved a length or two ahead of Valid Logic Systems Inc. However, in the first quarter of 1986, Mentor started pulling well ahead of the pack. Now it may be hard to dislodge Mentor from its strong position in the market.

MENTOR LEADS IN ELECTRONICS CAD/CAE SYSTEMS



TOTAL 1986 WORLDWIDE MARKET: $817 MILLION

SOURCE: DARATECH INC., CAMBRIDGE, MASS.

Although the market for design automation in the electronics industry is large and growing, it has not been smooth sailing for all participants. Mentor's business and financial status is on solid footing, however. No matter how secure a leader's position may seem, though, its management must worry about what could go wrong—and Mentor's management is no exception. One never-ending discussion at Mentor addresses the question of what hardware platform its applications should be built on, taking into account the rapid pace of computer development.

Mentor is the only company in electronic design automation to get through the 1985-86 recession in the electronics industry without layoffs or losses, maintains Tom Bruggere, chairman and chief executive officer. Mentor's current market share exceeds that of Daisy, Valid, and Tektronix combined (whose 1986 market share were 11.7%, 7.5%, and 1%, respectively), according to Mentor. Daratech Inc., a Cambridge, Mass., research firm specializing in the areas of computer-aided design, engineering, and manufacturing, confirms that Mentor's share of the electronics segment of the market was 21.2% in 1986, with the nearest competitor, Daisy, trailing with 11.7% (see chart).

Mentor is also moving up fast to the upper ranks of the total design-automation market. By the end of 1986 Mentor had captured the No. 6 spot in the revenue rankings for the total market, which includes big segments for mapping and mechanical, architectural, and construction engineering. Based on current estimates from Daratech, Mentor should move up to the No. 4 slot by the end of 1987, passing GE Co.'s Calma Co. and McDonnell-Douglas Corp. Mentor's share of the 1987 overall market will be 4.7%, with an estimated revenue of $208 million, according to Daratech.

In its first five years Mentor rapidly grew into a $174-million company with $11 million in profits for 1986. At the end of the first 1987 quarter Mentor's revenues were running at a $202 million annual rate. Quarterly net hit a record $4,174,000, a 120% increase over 1986's first quarter. Revenues rose 36% above 1986 to $50,498,000. Mentor's success is not a domestic-only phenomenon, either: it has captured a whopping 70% share of the electronics segment of the CAE/CAD market in Japan, for example.

Among the key corporate goals that Bruggere and Jerry Langeler, president and chief operating officer, have set out for Mentor is growth of 25% each year. "I see nothing to prevent Mentor from becoming a $1 billion company," says Langeler. "We think we have the management structure in place to grow to $1 billion. We have strong organizations in each critical area. But execution is what we have to watch most critically."

In a company on an sustained upward growth spiral, management cannot avoid thinking about where things could go wrong. Right now, Langeler and Bruggere worry less about their competitors than they do about what could happen internally. "There isn't anything a competitor can do that is worse than what we could do to ourselves," says Langeler.

"If we were to stumble on the implementation of the second generation of some products," says Bruggere, "that would hurt us." He is concerned about "the possibility of hurting a software product with future releases, or not getting a new product out on time."

But the management at Mentor is not myopic, either. Bruggere and Langeler still keep an eye on competitors. And Langeler points out that there is always the possibility that a fundamental structural change in the industry could occur. For example, he says, "The perceived value of a product that Mentor is offering could change out there while the cost of delivering it doesn't—that is a real problem."

From the start, Mentor's mission has been to help electronics companies improve their product-development process. The six major application areas that the company has identified include CAE and CAD, as well as computer-aided test, electronic packaging, publishing, and software engineering. The company has many application programs in its product line in each of these areas, except for computer-aided software engineering. "We don't know what [CASE] is yet," says Langeler.

Mentor currently has no plans to enter markets other than electronics. Electronic publishing, through its subsidiary Context Inc., is as far from conventional electronics as Mentor will go. Publishing design documentation is also important. "We see more than enough business in this [electronics] segment to

INTERNATIONAL NEWSLETTER

PHILIPS BESTS THE JAPANESE WITH ITS 1-Mbit STATIC RAM . . .

For the moment, the new speed and power record holder in the 1-Mbit static-RAM race is not from Japan—it's Philips of the Netherlands. The company says access time for the first working samples of its 1-Mbit CMOS static random-access memories is just 25 ns at 20 MHz. And dissipation is just 150 mW at 20 MHz during operation and less than 5 μW on standby. At this year's International Solid State Circuits Conference, Sony topped the list of 1-Mbit SRAM introductions with a chip that boasted a 35-ns access time at 100 mW. The Philips chip sports 0.7-μm minimum feature sizes and packs 128,000 8-bit memory locations onto a 94-mm² chip, making it the densest SRAM to date. Volume production is expected to begin in mid-1989. The Philips chip's small appetite for power should make it ideal for portable consumer equipment and battery-powered office systems. The development is part of the billion-dollar Mega Project, a joint effort by Philips and West Germany's Siemens AG to become top VLSI producers. □

. . . BUT SIEMENS ADMITS TO BIG PROBLEMS IN BUILDING ITS 1-Mbit DRAM

Siemens AG is having problems getting its 1-Mbit dynamic random-access memories to market. In a surprising display of candor, the Munich company admits that although deliveries were originally scheduled for the first half of 1987 [*Electronics*, Nov. 13, 1986, p. 30], it now has no firm idea when shipments will start. The 1-Mbit DRAM is one part of the Siemens-Philips joint memory effort, the Mega Project. The setback began when equipment Siemens needed for the new 1-Mbit fab line arrived late, but the situation appears to have worsened. The company now says that "still unsatisfactory yields and quality" are to blame for the delay. Company insiders say the problems may be due in part to the unproven equipment for handling the 6-in. wafers Siemens is using for the DRAMs. However, Siemens expects its integrated-circuit business to grow at more than a 10% clip this year, reaching about $440 million. □

FROM CANON AND INTEL, A CHIP THAT CONTROLS 10 FUNCTIONS AT ONCE

Canon Inc. and Intel Corp. are jointly developing an application-specific microcontroller around an Intel 80C51 core that will be capable of controlling 10 processes at once. The 80C51 will act as a supervisory unit at the center of 10 peripheral processing units, which will provide the equivalent of 10 controllers operating in parallel. Intel will fabricate the device in its CHMOS III process, and the two firms are negotiating to give the U. S. chip maker the rights to worldwide sales. Although the initial application is for an office photocopier, the chip is applicable to a wide variety of uses in office equipment and other electromechanical systems. □

SEIKO EPSON COLOR LCDs MAY REPLACE CRT DISPLAYS IN BOEING 7J7 JET

Seiko Epson Corp. is developing a color liquid-crystal display for use in the cockpit of Boeing Corp.'s next passenger jet, the 7J7, which is scheduled to make its first flight in 1990. Seiko Epson, of Suwa, Japan, is working with Rockwell International Corp., Pittsburgh, Pa., on the cockpit display systems for the jet, and they expect Boeing to adopt their design. Seiko Epson chose polysilicon thin-film-transistor technology for its color LCDs. The LCDs are better suited to the cockpit environment than conventional cathode-ray tubes, the company says, because LCDs use less power, do not wash out in bright sunlight, and take up less space than a comparable CRT. Seiko has not disclosed the dimensions of the new display, but the panel is believed to measure 7-in. square. □

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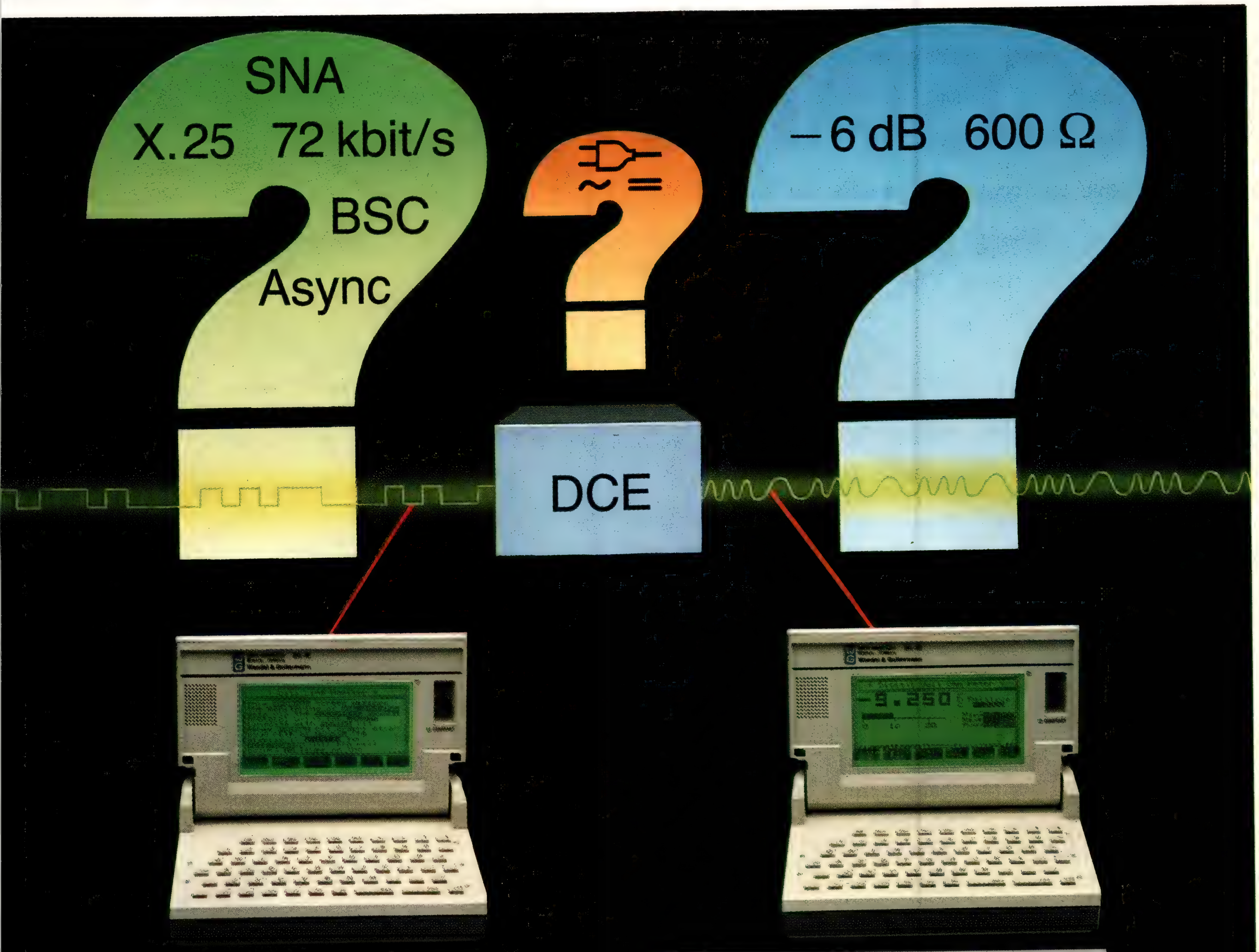

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INTERNATIONAL PRODUCTS

PHILIPS'S ADVANCED CMOS LOGIC BACKS TI'S NEW PINOUT SCHEME

1-MICRON PARTS RIVAL FAST BIPOLAR FOR SPEED AND DRIVE

By adopting a new pinout scheme in its 1-μm Advanced CMOS Logic family that rivals the speed and drive capability of the best TTL parts, Philips of the Netherlands has also achieved a threefold decrease in system noise, which reduces data-integrity problems encountered in high-speed switching.

With its ACL family, Philips has lined up with Texas Instruments Inc., Dallas, in the industry-wide pinout controversy. Philips and TI pioneered the new pinout, which moves voltage supply and ground pins from the corners to the center of dual in-line packages. It also adds a ground and supply pin for every pair of outputs, which means a 16-pin conventional DIP is replaced by a 20-pin part. TI introduced its first ACL parts in May [*Electronics,* May 14, 1987, p. 126].

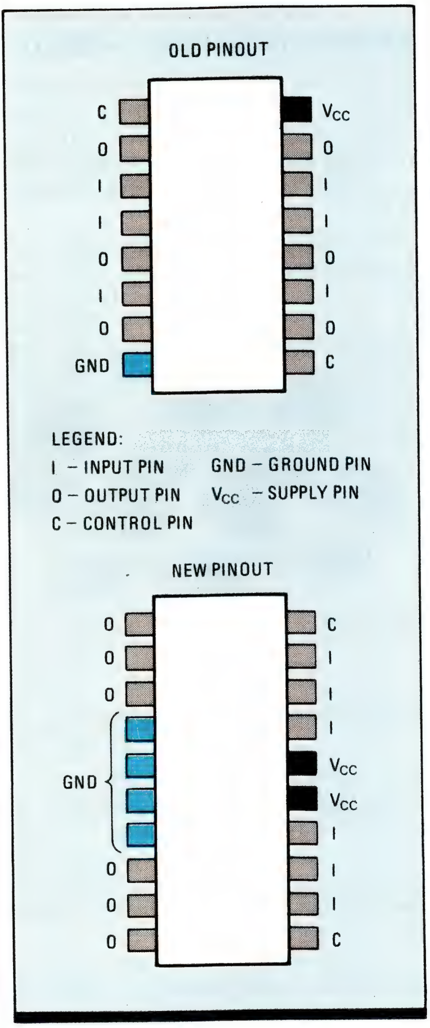
SWITCHING NOISE. Chip-to-pin lead lengths between the supply terminals play a major role in noise generation. Standard pinning maximizes lead length—and inductive noise—by placing supply and ground pins at diagonally opposite corners of the package. This creates problems in high-speed switching—lost data in internal flip-flops, extensive delays, poor noise immunity, and momentary changes of logic states.

Philips's parts, with their shorter lead lengths, avoid those problems. In a 14-pin DIP, for example, inductance drops from 10 nH for conventional pinning to 3.5 nH. Corresponding figures for a 24-pin package are 18 nH and 4 nH. Noise is cut threefold, from 2.5 V for a conventionally pinned device to around 0.8 V for an ACL center-pinned part.

The parts have an average propagation delay of 3 ns at a typical 150-MHz operating frequency and a 24 mA output—enough to drive 50- and 75-Ω terminated transmission lines, says the Dutch company.

Because the new pinout adds a ground and a supply pin for every pair of outputs, package size increases by about 10%. Better board design can compensate for this drawback.

The new pin arrangement "is the first attempt to bring the old-fashioned pinning for logic circuits in line with modern high-speed technologies," says Ad de Pagter, international product marketing manager for CMOS ICs at Philips's Electronic Components and Materials Division in Eindhoven. "With center-pinning, we know we are fighting a popular concept, but I think Jedec [the Joint Electron Device Engineering Council] will accept it as an alternate solution. In the end, the new configuration will win out."



CHANGES. Philips moved ground and supply pins to the center and added a ground and supply pin for each pair of outputs.

Many chip makers, notably in the U.S., oppose breaking away from two decades of packaging standards because doing so requires a different board layout. They argue that good design and, in the long run, greater use of surface-mount packaging will solve the problem of noise.

Philips contends that to exploit the speed potential of fast logic circuits, designers must use transmission-line techniques that require new board designs anyway. So obviously, says de Pagter, it is best to design ICs with the best pinning for high-speed ACL technology.

That technology should grab a big chunk of the logic market, Philips believes. According to market researcher Dataquest Inc., San Jose, Calif., TI and Philips together commanded one third of worldwide logic-device sales last year—$960 million of a total of $2.85 billion.

"ACL will spell an increase beyond the one-third level for the two firms," de Pagter predicts. By 1990, he thinks Philips will sell some $50 million worth of ACL parts worldwide.

CMOS PROCESS. The new family is based on a twin-well CMOS process with recessed local oxidation and a self-aligned titanium disilicide layer on the source, drain and gate areas. This reduces contact and interconnect resistance. Capacitance is reduced by oxide gate sidewall spacers.

With the effective transistor gate length just 1 μm, the on-chip propagation delay checks in at only 0.5 ns. The use of copper-doped aluminum interconnects on a tungsten layer minimizes electromigration. A p-epitaxial layer on a low-resistivity p-substrate makes the ACL family virtually latch-up free.

The typical quiescent power dissipation of an ACL gate is about 2.5 nW, roughly six orders of magnitude less than a bipolar gate. Dynamic power consumption is 0.18 mW at 100 KHz with a 50 pF load and a 5-V supply and increases to 180 mW at 100 MHz.

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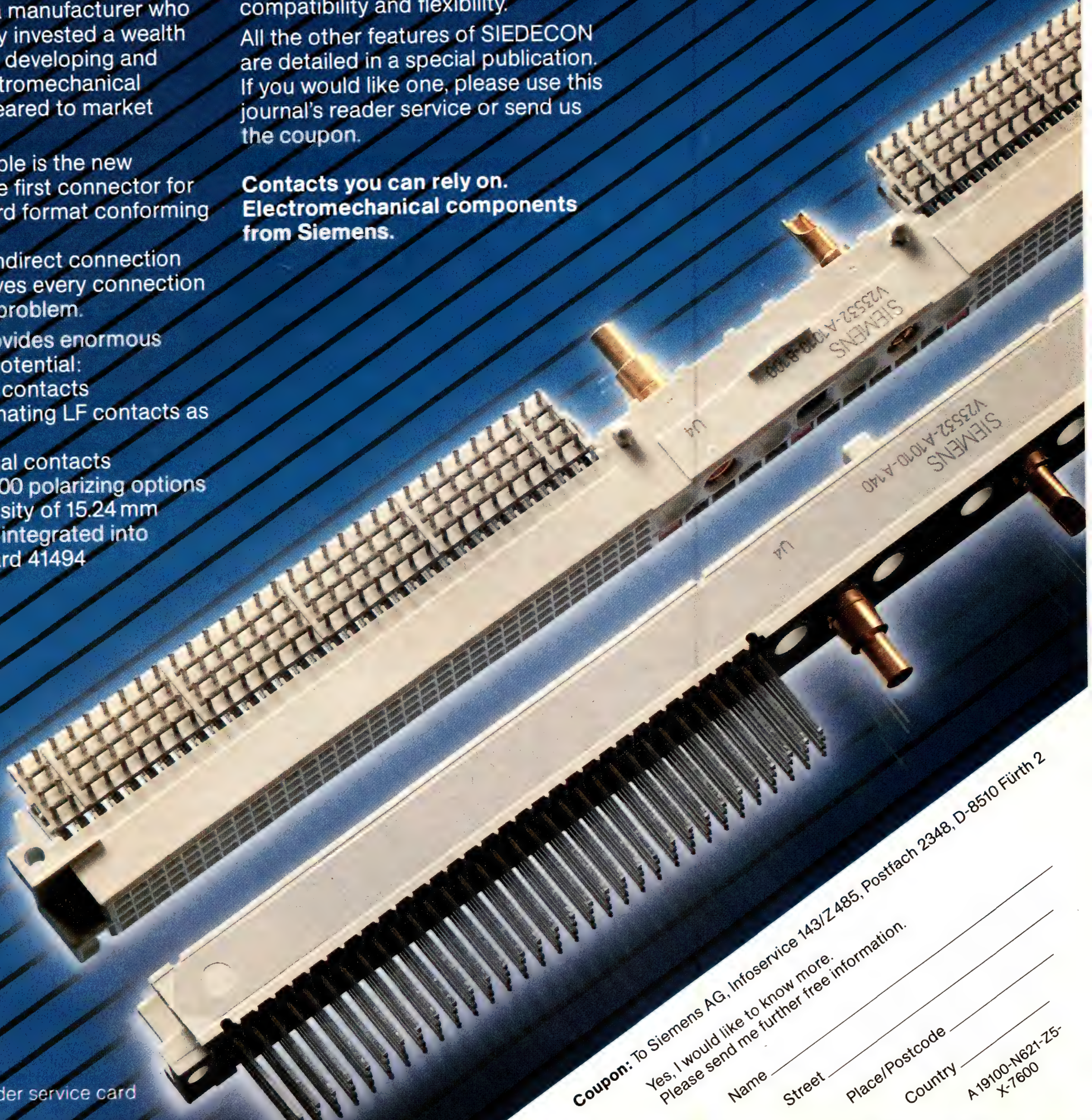

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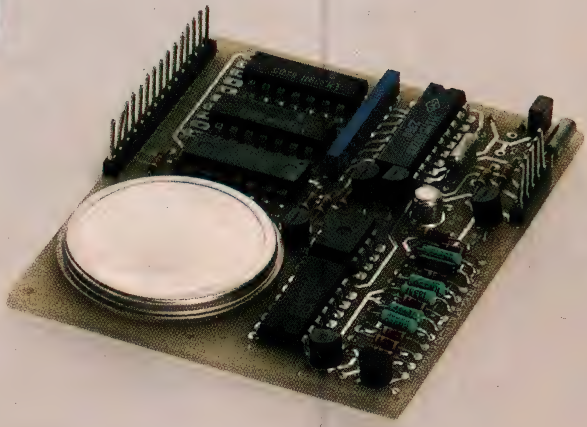

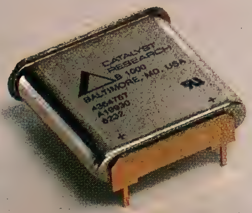

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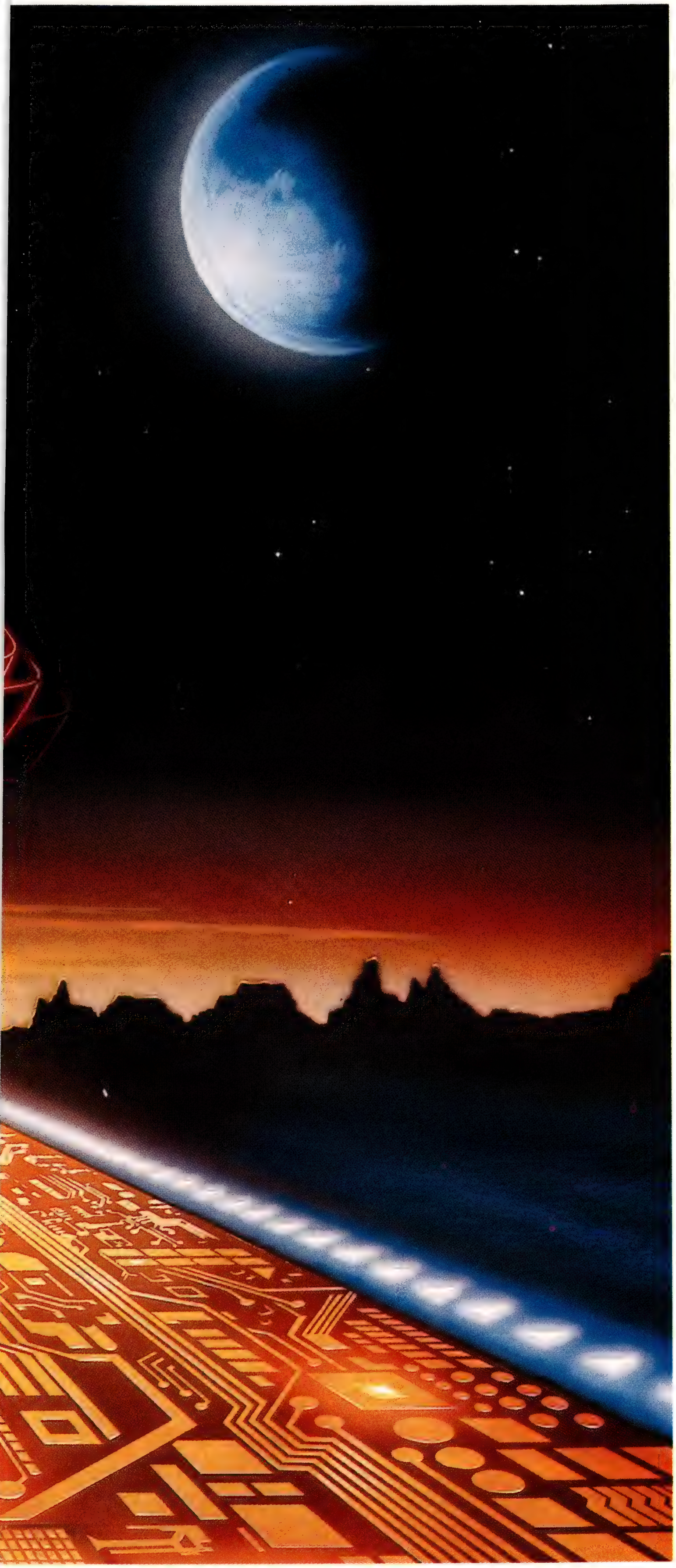

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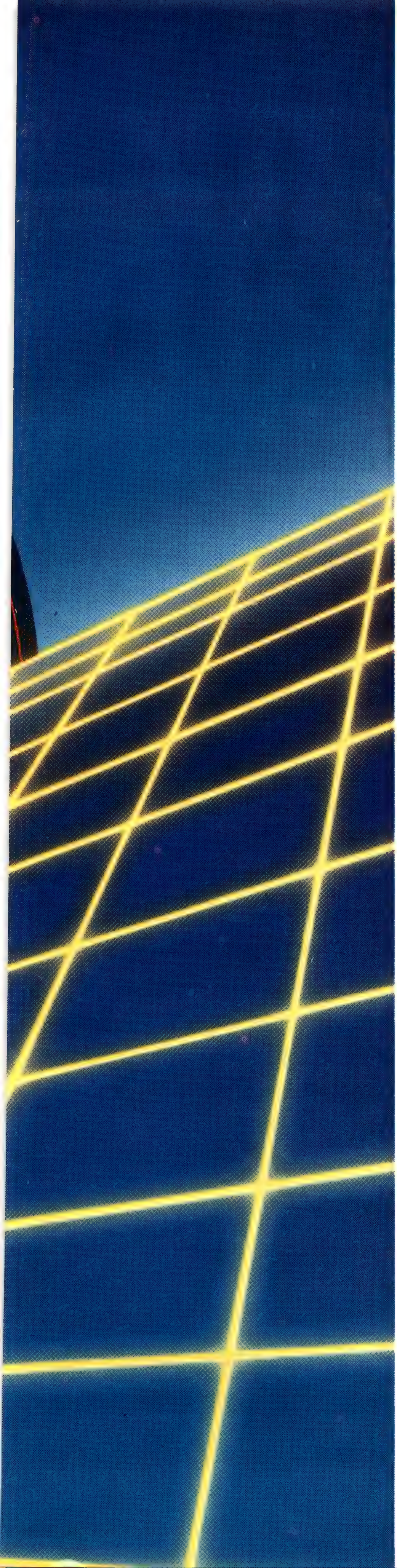

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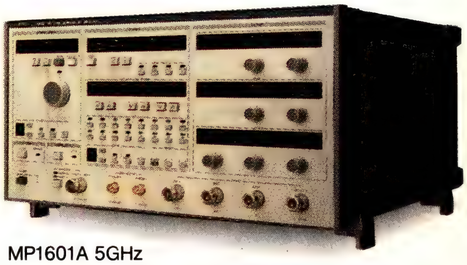

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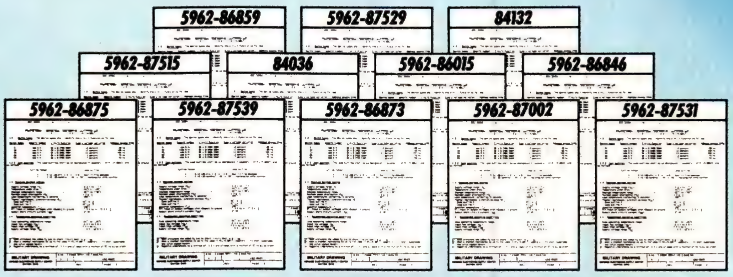
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THE CHANGING FACE OF NONVOLATILE MEMORIES

Faster, denser EPROMs and EEPROMs are finding new uses, displacing big ROMs and fast PROMs, for example; big chunks of them can also be added to ASICs

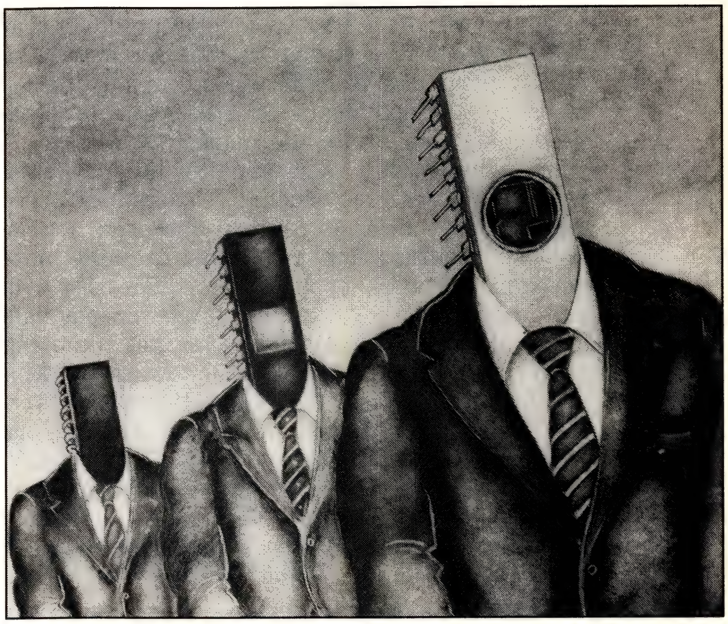
by Bernard C. Cole

Nonvolatile memories are taking on a whole new look. As both erasable programmable read-only memories and electrically erasable PROMs get faster and denser, they are starting to displace high-density ROMs and high-speed PROMs in new applications. In current applications, nonvolatile memory will now take up significantly less board space. Higher densities also will make it easier to incorporate larger amounts of nonvolatile memory on other types of chips, opening the door to logic chips that integrate large arrays of EPROM and EEPROM.

A new generation of higher-density commodity parts is under development, while lower-density parts are being pushed to significantly faster access times. Moreover, the need for designers to choose between speed and density may disappear, as companies such as WaferScale Integration Inc. in Fremont, Calif., (see p. 65) develop parts that combine both features.

Beyond making improvements to conventional parts, a drive is under way among chip makers to develop memories tailored to specific market segments—markets where speed is paramount, or power requirements are important, for instance. An example of the latter is a 64-Kbit EEPROM that needs only 3 V, reducing backup battery requirements in lightweight portable equipment. The part was jointly developed by Catalyst Semiconductor Inc. of Santa Clara, Calif., and Oki Semiconductor Corp. of Tokyo (see p. 67). In addition, companies are looking to incorporate nonvolatile-memory technology into other non-memory chips, applying their expertise to a variety of logic circuits—including microcontrollers, digital signal processors, programmable logic, and even application-specific integrated circuits based on standard cells.

One reason for all the activity in nonvolatile-memory product development is today's healthy market. The current crop of EPROM and EEPROM products are chalking up very strong sales—so strong that cautious manufacturers are reluctant to believe the optimistic projections of future business, says Victor deDios, senior industry analyst at Dataquest Inc. of San Jose, Calif. Overall, he says, worldwide EPROM sales for 1987 can be expected to hit $1 billion, up 8% from $910 million in 1986 and up 14% from the reces-



Mike Villott, vice president of marketing at Seeq, and they provide EEPROM features previously not available. Such features include on-chip address and data input latches to permit microprocessor-compatible write and erase cycles, as well as chip-erase and page-erase modes.

And whereas the 48128 required a 21-V power supply on multiple pins, the new flash EEPROMs require only a single 12-V external supply for programming and erasure. Moreover, he says, this programming voltage can be applied during read operations, which eliminates the need to switch it off when not erasing or programming. Byte write time is only 1 ms, and chip and byte erase times are no more than 5 s. Endurance—the number of times the device can be erased and written to—is 100 cycles minimum and can be screened to 1,000 cycles.

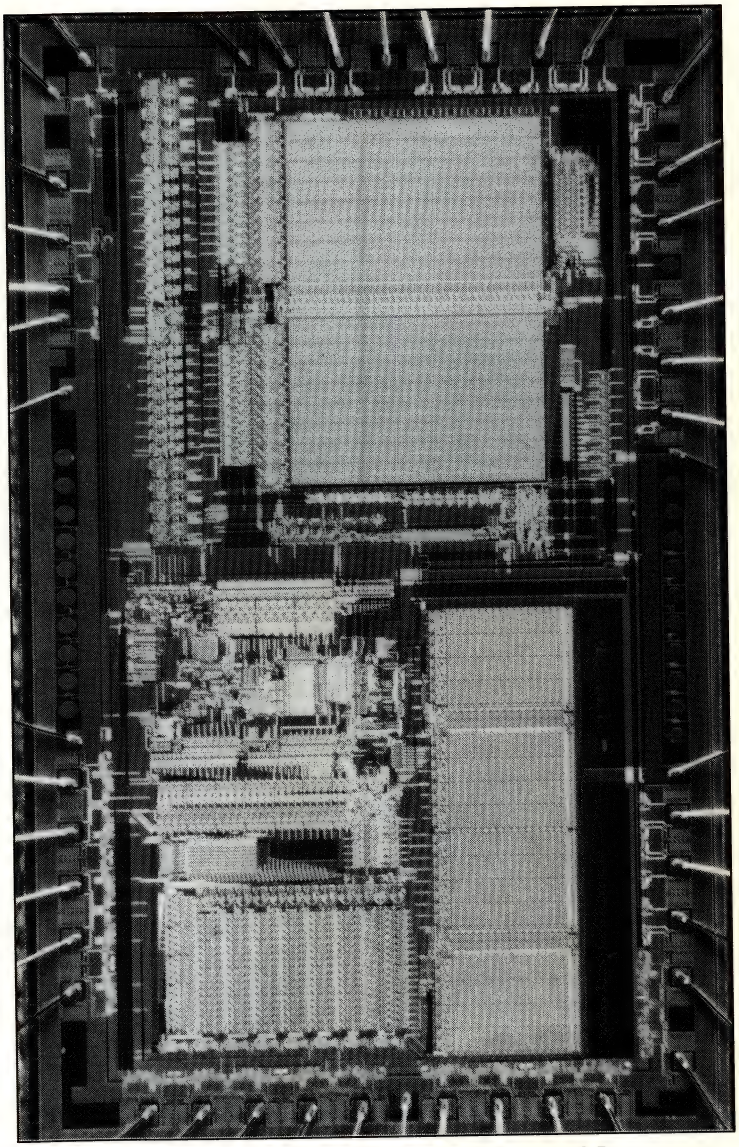
Hoping to follow Seeq into the market with a high-density flash EEPROM is Exel Microelectronics of San Jose, Calif., which is in development on a 512-Kbit device it expects to introduce early next year. Also investigating the technology as a way to achieve higher EEPROM densities are AMD, Fujitsu, Hitachi, National Semiconductor, Texas Instruments, and Toshiba.

Another recent convert appears to be Intel Corp., Santa Clara, Calif., although until recently it was enthusiastically exploring another approach to high-density EEPROMs, the thick-oxide technique pioneered by Xicor Inc. of San Jose, Calif. Intel, however, has abandoned its efforts in this area, says Don Knowlton, general manager of Intel's programmable-memory operations in Folsom, Calif., and is investigating other techniques for higher density, including the flash-EEPROM approach.

That leaves Xicor going it alone with the thick-oxide technique. The company is now in production with a 256-Kbit n-MOS device, the X28256 [*Electronics,* May 12, 1986, p. 30] and is also developing a CMOS version, the X28C256, which it expects to introduce later this year, and a 1-Mbit device tentatively scheduled for early next year.

For many manufacturers, however, the bright prospects in the mainstream EPROM and EEPROM market are essentially an opportunity to carve out new niches. The past has taught them a painful lesson: the memories may be nonvolatile, but their market is not. They want to find areas where price pressure and competition are less intense. Among the possibilities they're exploring are high-speed bipolar PROM replacements, parts tailored to specific applications such as smart cards, and other applications outside the traditional domain of EPROMs and EEPROMs.

Two companies that have successfully established themselves in the bipolar PROM replacement market are Cypress Semiconductor Inc. of San Jose, Calif., and WaferScale Integration, with 16-Kbit and 64-Kbit CMOS EPROMs in the 35-to-50-ns range. Also looking to participate is Seeq, which has just introduced two byte-wide 35-ns EEPROMs, the 16-Kbit bit 36C16 and the 32-Kbit 36C32 [*Electronics,* April 30, 1987, p. 66]. Others thinking hard about entering the market include AMD, Intel, and SGS.



2. REPROGRAMMABLE DSP. General Instrument has put 2.5 Kbytes of EEPROM on a digital signal processor chip.

Another niche is being explored by Intel, which is looking at what Knowlton calls "application-oriented" EPROMs—nonvolatile memory devices with extra logic that optimizes the devices for specific applications. One of the company's first efforts in this direction was the 27916 KEPROM, or keyed-access EPROM, which combines the memory array with a pseudo-random number generator and encryption circuitry that can determine if the person accessing its contents is authorized. Taking the concept even further, the company this month introduced the first in a new series of such applications-oriented EPROMs, the 87C257 and 68C257—256-Kbit devices with on-chip latches that allow the memory's address and data pins to be tied directly to a microcontroller's multiplexed address and data

WAFERSCALE'S 256-K EPROM RUNS SUPERFAST

Speed or density? Density or speed? Thanks to WaferScale Integration Inc., systems designers no longer must compromise. The Fremont, Calif., company has just unleashed a pair of high-speed, 256-Kbit ultraviolet-erasable CMOS programmable read-only memories. With 50- to 55-ns access times, they are the fastest nonvolatile memories on the market at 256 Kbits and beyond—at least two to three times quicker than comparably sized PROMs, and coming within range, at twice the density, of the largest commercial bipolar PROM [*Electronics*, Feb. 10, 1986, p. 35]. And active power dissipation is a comfortable 325 milliwatts, just half that of its closest bipolar rival, sinking to 75 mW on standby.

With their combination of speed and density, the word-wide 16-K-by-16-bit WS57C257 and byte-wide 32-K-by-8-bit WS57C256F are tailored to one- and two-chip program storage for 16- and 32-bit microprocessors and digital signal processing. Conventionally, anywhere from 4 to 16 nonvolatile memories are needed. Current plans call for the byte-wide memory to hit the streets in July in standard 28-pin ceramic dual in-line packages and 32-pin ceramic leadless chip carriers. The word-wide part will follow sometime in the third quarter, in 40-pin Cerdips and 44-lead ceramic leadless chip carriers. Both are priced at $94 per unit in 100-unit sample quantities.

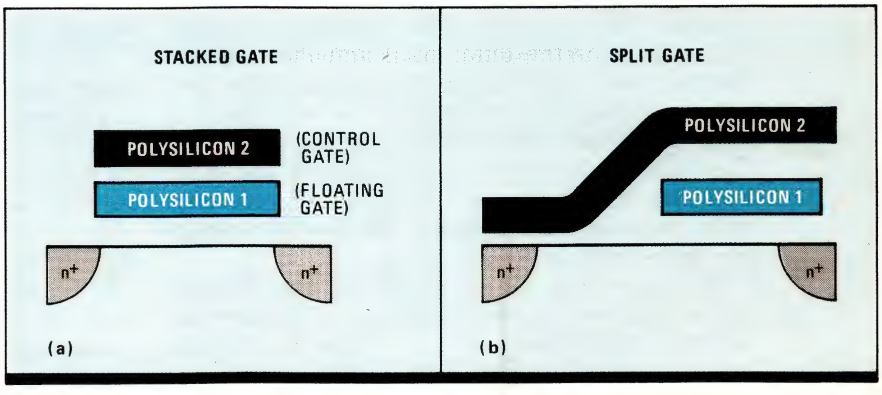
To achieve this unprecedented combination of speed and density, engineers at WaferScale Integration refined the company's process technology and fine-tuned the circuit design. On the process side, a slimmed-down, second-generation 1.2-μm CMOS process, a scaled version of the company's patented split-gate EPROM cell, and tungsten silicide word lines were the keys to success. On the circuit-design side, clocked differential sensing and a novel precharge technique, a special two-step ac signal scheme, and address-transition detection were the key developments. "These two devices disprove the traditional belief that you could have speed or size, but not both, in your microcontrol store," says Jerry Banks, marketing manager for standard products. "These large-architecture CMOS EPROMs are ideally suited for modems, real-time control, guidance systems, digital signal processing, and other real-time or complex processing applications."

WaferScale Integration first boiled down its CMOS process—from 1.5 to 1.2 μm—and then used the refined technology to whip up a scaled version of its proprietary split-gate EPROM cell. Just 6.5 μm on a side, the latest split-gate incarnation is roughly half the size of its predecessor. There's more to the new cell than just size, but the company won't go any further than saying that it adopted tungsten silicide.

The main problem with the traditonal stacked-gate cell, notes Boaz Eitan, manager of the PROM program, is that it forces a tradeoff between the necessarily high read current and efficient programmability. "In traditional implementations, chip designers have had to make a choice," he says. "If they wanted speed, they had to implement a PROM cell with three to four transistors, separating the read, write, and select functions. If they wanted density, all three functions could be incorporated into a single-stacked PROM cell, but only at considerable sacrifice in speed."

The heart of the trouble lies in rapidly sensing the word- and bit-line voltages after address decoding. "The bit-line capacitance plays a big part in the equation," explains Syed Ali, manager of memory design. "If the capacitance remains fixed, a higher read current is needed to achieve greater speed. However, if the capacitance can be lowered, the speed can be boosted without increasing the read current."

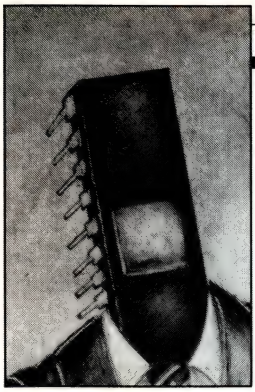
The split-gate structure weds the best of the multiple-transistor and single-stacked cell approaches, requiring none of the compromises inherent in either. It consists of a MOS transistor linked in series with a floating-gate transistor that has been merged into a composite device (see fig. 1). In this design, says Eitan, the second polysilicon layer acts as the control gate and directly covers part of the channel area. "This eliminates drain turn-on and source-drain punchthrough, which adversely affects the stan-



1. SPLITS. Unlike the stacked-gate transistor (a), the split-gate transistor (b) has a second poly control gate that partly covers the channel, preventing drain turn-on and source-drain punchthrough.

TECHNOLOGY TO WATCH

CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS



Five volts is no longer the magic number when engineers talk portable and battery-backed applications. Catalyst Semiconductor Inc. of Santa Clara, Calif., has just put the finishing touches on a 64-Kbit EEPROM that reads and writes with a supply voltage as low as 3 V. And this diminutive appetite comes at no substantial cost in speed. With an access time of 120 ns, the memory keeps pace with many existing 5-V devices. When operated at 5 V, its reads take a mere 60 ns. Also in its favor is the fact that it draws an active current of only 7.5 mA at 8 MHz, about a fifth that of its rivals.

Low voltage opens up a wide range of battery-backed applications, says B. K. Marya, Catalyst's founder and president—among them, hand-held computers, smart cards, pagers, beepers, and many telecommunications devices, which require long-term battery backup as well as small size.

The memory also will compete with nonvolatile static random-access memories that incorporate a 3-V lithium battery. "The advantage of battery-powered nonvolatile SRAMs is their ability to read and write data with access times of 120 ns or less," Marya points out. Moreover, "traditional high-density EEPROMs of 64 Kbits or more usually require at least a 5-V read and write voltage. And they are not only slow but also difficult to operate if reprogramming is necessary, requiring as they do at least four AA-type batteries or an expensive lithium power source." Because it can be operated and programmed with a 3-V supply, the device requires only two 1.5-V batteries in portable consumer settings and makes it possible to go with small lithium power sources in smart cards. Eventually, Marya says, as the power-supply requirements of EEPROMs continue to decline, it may be possible to substitute solar cells for batteries in a wide variety of applications.

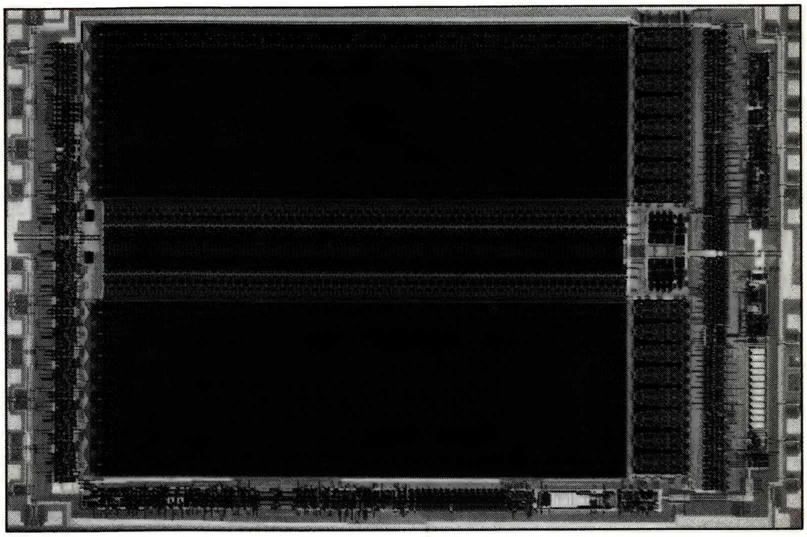
The EEPROM is the fruit of international cooperation. The cell and circuit design were contributed by Catalyst, which also created and modified the architecture. Oki Semiconductor of Tokyo furnished the process, jointly modified by the two partners, and served as the silicon foundry.

Critical to the success of the joint venture was a variety of proprietary circuit wizardry. Broadening the supply-voltage range ensured successful reads and writes despite voltage fluctuations. Bootstrapping capacitors and a clever differential sense amplifier make certain that reads are accomplished quickly in the face of low voltage and power-supply variations.

In addition, a dual-clocked, high-voltage switching circuit guarantees that switches are thrown reliably, even when the voltage fluctuates. And dynamic, rather than static, page latching keeps the memory writing even while supply voltage varies.

Measuring 4.84 by 7.06 mm and housed in a 28-pin plastic dual in-line package, the Catalyst MSM28C64A (see fig. 1) is fabricated with a slight modification of Oki's 1.5-μm n-well double-polysilicon CMOS floating-gate process. The memory incorporates five types of transistors: p-channel and n-channel enhancement-mode MOS transistors for fabricating the 3-V circuits, and enhancement, depletion, and non-ion-implanted n-type transistors for fabricating the charge-pumping circuitry that converts the 3-V supply to 18 V on-chip; in addition to these transistors, there are the floating-gate devices themselves.

The key to achieving low-voltage operation in portable applications is the ability to maintain stable reads and writes over long periods, despite the substantial variations in supply voltage associated with batteries. Relaxing the supply-voltage tolerances of the basic EEPROM cell makes that possible. With its dynamic page-mode latching scheme, the device is relatively insensitive to voltage changes and can operate even if the supply voltage varies 20% in either direction, Catalyst claims. By comparison, most competitive devices can operate only within variations of ±10 V. When operated at, for example, 5 V, the Catalyst part's supply voltage can vary from 4 to 6 V, whereas conventional EEPROMs



1. LOW VOLTAGE. Catalyst's MSM28C64A EEPROM has five types of transistors that form the charge-pump circuit needed to convert the 3-V supply to 18 V on-chip.

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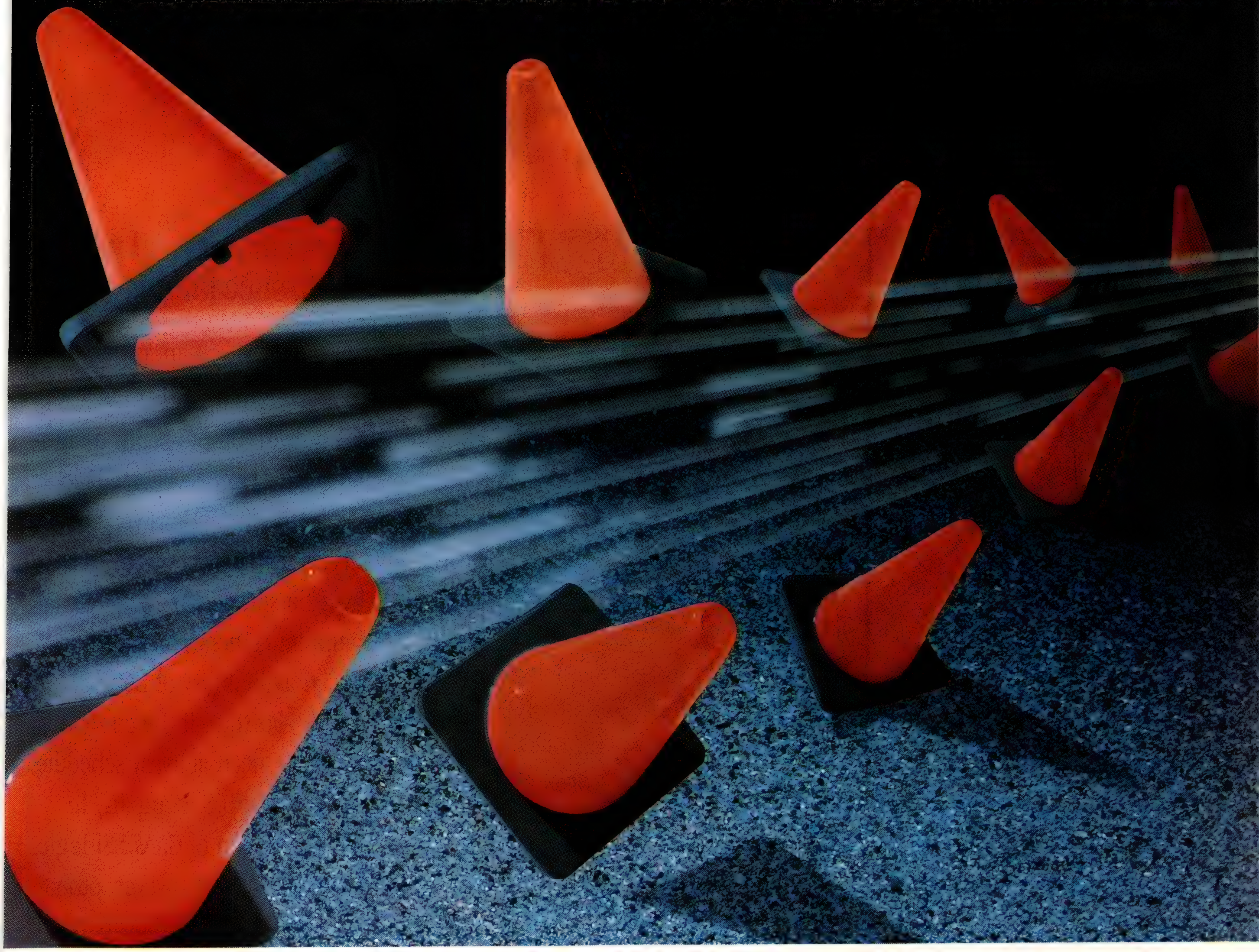

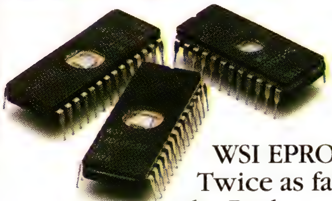

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WS57C128F	70 ns.	16k x 8 CMOS EPROM
WS57C256F	70 ns.	32k x 8 CMOS EPROM
WS57C65	55 ns.	4k x 16 CMOS EPROM
WS57C257	70 ns.	16k x 16 CMOS EPROM

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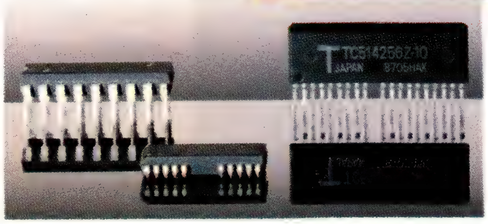

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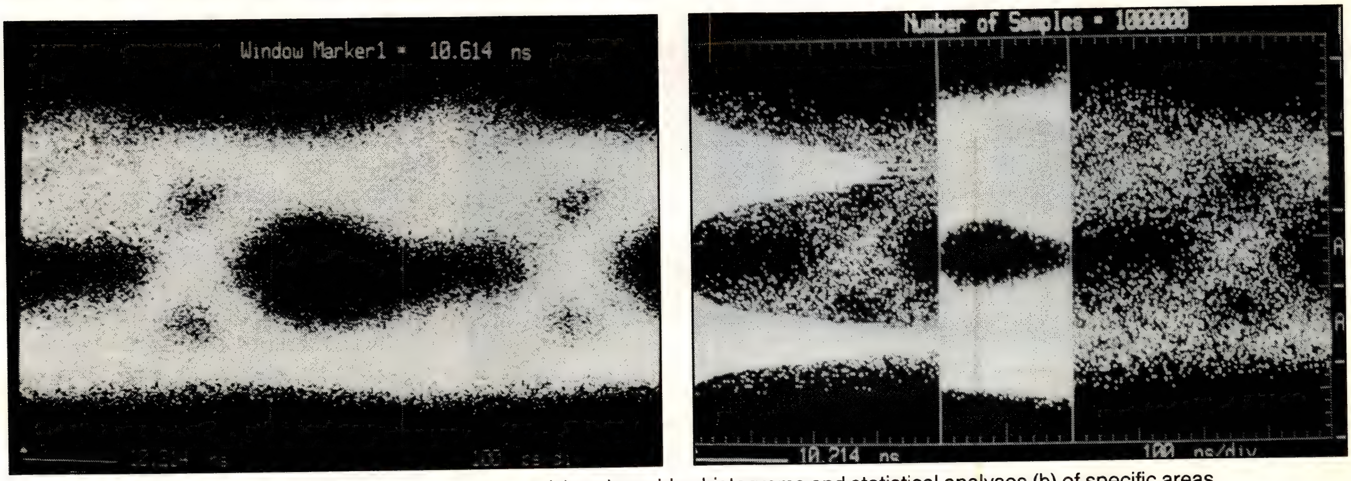


2. PATTERN ANALYSIS. The scope displays eye patterns (a) and provides histograms and statistical analyses (b) of specific areas. These statistical analyses of an eye pattern show both timing and amplitude variations for an area of the pattern.

rameters and helps the calibration subsystem null the effects of interconnections between scope inputs and measurement points. And new probes simplify measurement of high-impedance designs.

Besides automating many wideband measurements, the 54120T automates analysis. The scope has a persistence mode to hold fine details of waveforms on the display and to emulate variable-persistence analog scopes. In this mode, for instance, a user can build up a traditional eye pattern—a hole surrounded by gray shades created by the noise and jitter of multiple waveforms. But instead of estimating amplitude and timing variations, he can view histograms and statistical analyses of specific areas of the patterns (see fig. 2).

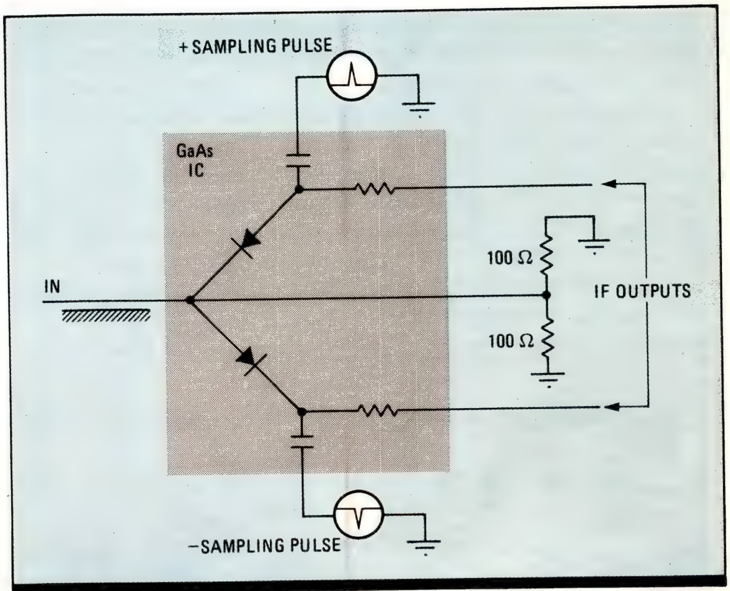
A 20-GHz digital sampling scope is not a breakthrough in speed. Earlier this year Hypres Inc., Elmsford, N. Y., introduced a 70-GHz system that samples up to four channels through liquid-helium-cooled Josephson-junction circuits [*Electronics*, Feb. 19, 1987, p. 49]. However, Hypres' system costs five or six times as much as the 54120T: $120,000 for a mainframe, plus $20,000 to $45,000 for input modules.

The 54120T costs $1,000 less than the widest-band configuration of the leading sampling scope—Tektronix Inc.'s dual-trace 7854 with 14-GHz sampling and reflectometer modules, but without accessories. However, the 7854 mainframe is also a 400-MHz real-time scope with digital waveform processing that can be used with other modules in other applications, whereas HP's 54120T reaches higher sampling bandwidth and precision by focusing sharply on its own applications range. Because the 54120T got its 20-GHz repetitive bandwidth by abandoning the single-shot mode that enables digitizers to capture a single waveform, it cannot compete with analog scopes in traditional real-time applications.

HP's goal was to be able to analyze pulse rise times, settling times, and step perturbations that in the past were too fast to measure. So it redeveloped an old, slow sequential-sampling architecture with microwave-analyzer circuitry. The circuitry lets the 54120T take a single sample at a time from repetitive waveforms and record the overall waveform as a straightforward sequence of data points at rates around 5,000 samples per second. Other HP digitizers reach single-shot bandwidths of up to 250 MHz with a billion samples/s, but they have lower resolution and don't go beyond 1 GHz in repetitive bandwidths.

Each channel in the 54120T samples up to 512 repetitive waveforms. The sampling rate is paced by the input repetition rate: an external trigger signal comes in at the start of each waveform, and the sampling time is delayed by a precision timing circuit. Sample timing is programmable, so automated measurement of mixed-waveform runs can be performed.

To remove unwanted skews from the measurements, delays between channels are adjustable in 1-ps steps. For measurements requiring precision stimuli, channel 1 contains a step-recovery-diode circuit that puts out 35-ps step pulses and offsets



3. KEY CHIP. A gallium arsenide step-recovery-diode bridge from an HP microwave network analyzer operates as a narrow-aperture sampling gate.

TI'S TRENCH TECHNOLOGY MOVES INTO THE FACTORY

After getting control of this tricky etch process, TI turns out 1-Mbit DRAMs with trench capacitors; researchers use it to boost PROM densities and isolate bipolar devices

When builders want to squeeze more out of a piece of real estate, they have only one way to go: up. But developers of silicon real estate have been going in the other direction. To pack more functions into a given VLSI area, device designers are working on a three-dimensional vertical-integration process called trench etching, in which holes or grooves are etched down into a chip's substrate and used for either isolation or device fabrication.

But trench etching hasn't yet moved into the factory, because it has been too tricky a process to meet the throughput demands of full production. Now, however, researchers at Texas Instruments Inc. have come up with a new technique that provides better control of the etch process, allowing them to bring trench technology to the VLSI production line for use in 1- and 4-Mbit dynamic random-access memories.

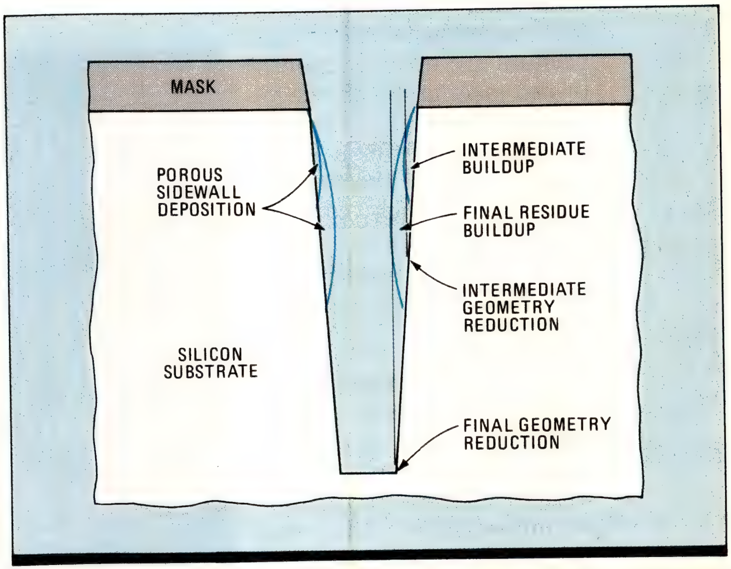
The additional chip area provided by trenching can be used to construct simple active devices or to establish area-efficient device isolation without the latchup-inducing encroachment problem inherent in conventional isolation techniques. A trench can also be used to place an insulating barrier or a conductive interconnect between a chip's surface and buried layers.

The Dallas chip maker is already turning out 1-Mbit DRAMs with trench capacitors. A forthcoming 4-Mbit DRAM will go even further, placing a storage capacitor, a transfer gate, and a contact into the same trench. What's more, TI researchers recently achieved improved programmability, better device isolation, and reduced parasitic capacitance in erasable programmable read-only memories by using a novel positioning of trench isolation between bit lines and transistors; this approach should move bit-line spacing below 1 μm. The researchers are also using trenches to isolate devices on advanced bipolar circuits.

Several problems have hampered trench technology, including undercutting of the mask and grooving at the trench bottom during the etching process. Undercutting promotes the formation of voids during subsequent refill of the trench, and contaminants can easily get into the voids and cause reliability problems. Grooving, or the formation of a V-shaped structure on each side of the trench bottom, can degrade the dielectric integrity of a trench capacitor and can promote stress-related silicon defect densities during thick thermal oxidation.

TI's selective sidewall deposition technique counters these problems by precisely controlling the profile of the trench as it is etched so as to achieve the surface texture and dimensions required to make trench technology a viable production process. TI uses a dry-etch process and produces a trench that has straight, unbowed walls and is free of defects on its floor.

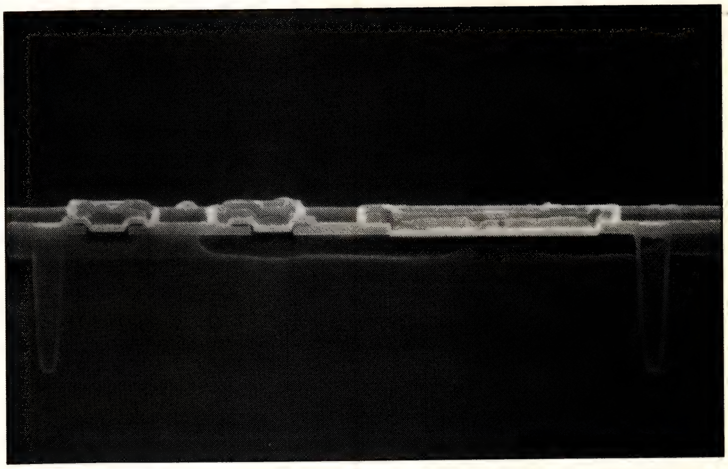
The new technique involves selective deposition of etch products on the trench's sidewall near the mask/silicon interface by two means: controlled forward sputtering of the mask material and condensation of gas-phase precipitates formed in the reactor. The deposits protect the upper sidewall from erosion (see fig. 1) and are



1. PROFILE. In Texas Instruments's trench-etch technique, etch products are selectively deposited on the trench sidewalls to protect them during deep etching.

slope, ±0.5°, to enhance capacitance and to prevent sharp terminating points. A capacitor formed this way exhibits well-behaved electrical characteristics for gate and drain voltages above 5 V, Douglas says.

Advanced bipolar devices use trenches mainly for device isolation. As with DRAMs, the aspect ratio must be high: a 15-μm depth for a 2-μm trench width or an 8-μm depth for a submicron width. Smooth sidewall surfaces with ±1° slope control are required. Isolation trenches lay out as long slots, rather than as "postholes," and are usually easier to etch. Whereas tank-to-tank spacing of 10 μm is currently in production with oxide isolation, trench isolation allows this dimension to shrink to 2 μm and substantially increases the packing density of bipolar devices. Trench isolation also eliminates the need for a channel stop under the field oxide, significantly reducing the collector-to-DUF (diffusion-under-film) capacitance (see fig. 4).



4. DENSE BIPOLAR. Tank-to-tank spacing in bipolar devices can be reduced from 10 μm with oxides to just 2 μm with trenches.

In another isolation application, a 15-μm-deep trench-isolated SIMOX (separation by implanted oxygen) structure can replace standard dielectric isolation to achieve higher packing density and increased immunity to radiation effects.

To obtain reasonable throughput on a production line, the etch rate in the trench process must be at least twice as fast as in other processes, since the vertical depth to be etched is some 5 to 50 times greater than the thickness of films etched in conventional processes. This fact has demanding ramifications in mask selectivity, critical-dimension control, and other variables.

With trench etching, surface texture and damage considerations during production are more significant than in other dry-etch processes, because the trench-etched surface is generally destined to be an active silicon area, or at least a turned-off parasitic device in the final circuit. Newly created surfaces must be suitable for building active-device components. Because of the highly directional etch conditions, micromasking and other effects contribute to surface asperities. Without sidewall deposition, ion bombardment would result in silicon lattice damage.

When it came to choosing a means of production, the TI researchers found a single-wafer reactor to be far superior to batch reactors for trench-etch processing. "Batch reactors are more expensive than single-wafer systems; they exhibit poor selectivity to photoresist as an etch mask; and they are plagued by large etch-rate and trench-profile nonuniformities," says Douglas. "In addition, they are difficult and somewhat dangerous to clean and, as wafer size increases, it becomes more of a fiscal liability to commit a whole batch of wafers to a single run." Not only do the long run periods make it it difficult to develop a process in a batch reactor, but it is also expensive and time-consuming to requalify all wafer positions on a batch system, he adds. These require exhaustive analysis with a scanning electron microscope.

TI researchers chose to engineer their own single-wafer reactive ion etching reactor. This reactor etches silicon faster than 2.5 μm per minute and has better than 150:1 silicon-to-oxide and 40:1 silicon-to-photoresist etch-rate ratios, all with good profile control. ☐

For more information, circle 483 on the reader service card.

THIS CHEMIST GETS DOWN INTO THE TRENCHES

It's been a life in the trenches, so to speak, for much of Monte Douglas's past five years at Texas Instruments Inc. As a senior member of the technical staff at TI's Semiconductor Process Laboratory in Dallas, he's pioneered techniques for etching deep silicon trenches for advanced device applications in dynamic random-access memories, advanced bipolar devices, erasable programmable read-only memories, and CMOS parts.

Douglas, 31, holds a BS in chemistry from Nebraska Wesleyan University and a PhD in physical chemistry from Rice University. He has more than 15 patents issued or pending. At TI, he is also involved with the development of new plasma chemistries and in designing reactor hardware for dry etching of a variety of new materials that will be required for ultra-large-scale integration. He is currently at work on dry-etch techniques for salicide local-inteconnect technology for advanced static RAMs.

Douglas's work in trench technology is an essential part of a forthcoming 4-Mbit DRAM and will play a big role in future ultra-large-scale-integration devices, says Greg Armstrong, associate director of the lab. "The problem in big DRAMs is to get sufficient capacitance in a reasonably sized chip. The only way to do that is to go vertical."

Trenches are already being used in TI's production 1-Mbit DRAMs. "For these chips, the trenches only have to be 3 to 4 μm deep," says Armstrong. "At 4 Mbit, they'll have to be 7 to 9 μm. Control of the trench profile at that depth is a real challenge." But he believes the selective-deposition technique TI is successfully using to make its 1-Mbit DRAMs gives the company an advantage when it comes to that challenge.

MONTE DOUGLAS

WHAT'S NEW IN INTERCONNECTIONS?

THE IC SOCKET GETS NEW LIFE FROM THE VLSI CHIP

A variety of complex sockets are being developed to handle expensive VLSI chips, avoiding the risks of soldering ICs with 100 leads or more directly to a pc board

by Jerry Lyman

The integrated-circuit socket is grabbing the spotlight in interconnections, thanks to the arrival of production VLSI chips with more than 100 leads. Up until recently, IC sockets were used mainly to make it easier to repair or replace packages with few leads in systems that needed frequent field servicing or hardware updates. Now designers need a way to overcome the risks in soldering multileaded ICs directly to a printed-circuit board. So packaging designers are devising a variety of complex sockets to house expensive VLSI chips with hundreds of leads on tightly packed centers, typically 25 to 50 mils.

Packages with many leads are difficult to solder onto a fine-line pc board. And removing such a device without damaging an expensive pc board is even harder when it is soldered in place. This is where complex sockets play a leading role. Sockets allow easy modification of a board because a gate array or other type of programmable ASIC can be simply replaced with an updated device.

The special high-temperature sockets required for burn-in or high-temperature screening of ICs represent another large application. And designers are using new materials such as engineering thermoplastics and liquid-crystal polymers to overcome the temperature and mechanical stresses of surface mounting, a technique that is growing in popularity. These new sockets will take up more space than a soldered IC, but in the long run they will also result in increased board yield.

Most IC sockets are used by the computer-manufacturing industry, which in 1986 accounted for 72% of all sockets sold in the U. S. Computer manufacturers should continue to dominate socket sales (see table, right). And their growing usefulness will keep IC sockets a growing market segment. Last year, they made up 6%, or $247 million, of the nearly $4 billion worth of connectors used in the U. S., and the market for sockets is projected to grow to $300 million by 1991 at an average annual growth rate of 4% (see table, next page).

Packaging designers and socket manufacturers currently face a bewildering array of IC packaging choices, which in turn leads to a variety of socket types. Packages include the dual

COMPUTERS LEAD U.S. CONSUMPTION OF IC SOCKETS

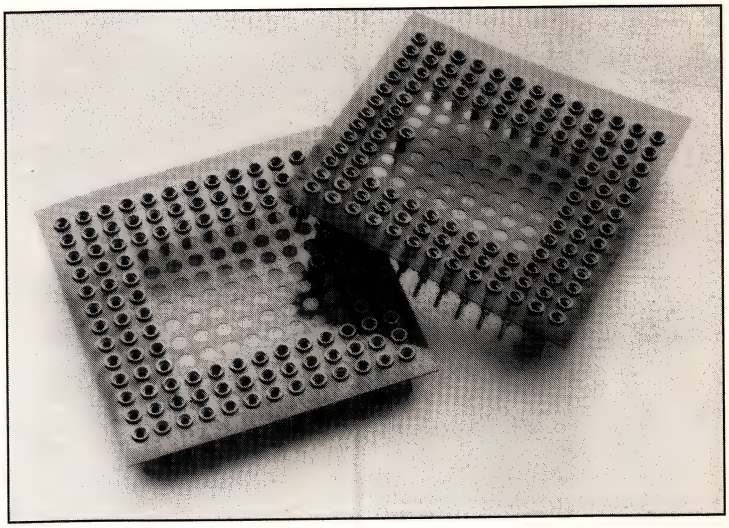
Electronic equipment category	1986 ($ millions)	1991 ($ millions)	Average annual growth (%)
Electronic			
Computer	178	219	4.2
Communication	26	35	6.7
Government/military	18	17	−1.3
Instrumentation	6	7	1.3
Industrial	6	6	0.3
Consumer	3	5	6.1
Business/retail/education	3	3	1.3
Electrical/industrial			
Transportation	4	5	4.2
Machinery	3	3	4.3
Total consumption	**247**	**300**	**4**

Dollar figures have been rounded to the nearest whole number

SOURCE: GNOSTIC CONCEPTS INC.

in-line plastic package with staggered leads on 100-mil centers that several Japanese companies started delivering late last year. Advanced Interconnections, Amp, Augat, and Garry are working on these sockets. Molex Inc. of Lisle, Ill., was first to produce a SIMM connector for a vertical package, a configuration originally requested by Wang Laboratories Inc. and developed by TI. The SIMM consists of a small pc board with arrays of memory chips in plastic leaded chip carriers on both sides. The input and output leads of the module are plated-edge card fingers placed along one of its long dimensions on 50- or 100-mil centers. Now Amp Inc. (see fig. 1) and Burndy Corp. of Norwalk, Conn., are also producing these sockets, which can have up to 68 leads. Molex is already receiving requests for sockets designed to accept SIMMs with edge-card fingers on 25-mil centers.

Another alternative for high-density packaging is the plastic leaded chip carrier, but its practical maximum is 84 leads. Nearly all the connector-manufacturing companies now have sockets for this package, which has J-leads on 50-mil centers. The only question for a potential user is whether to use a surface-mount or through-hole version of the socket. So far, about 80% of all plastic-leaded-chip-carrier sockets are being through-hole mounted. Nearly all the surface-mounted versions use the gull-wing configuration, usually on staggered 100-mil centers, for the socket leads.



2. PIN PATTERNS. Augat's PKC series has PGA pin patterns in polyimide carriers. After soldering, the film is removed.

PIN GRIDS OR FLAT PACKS?

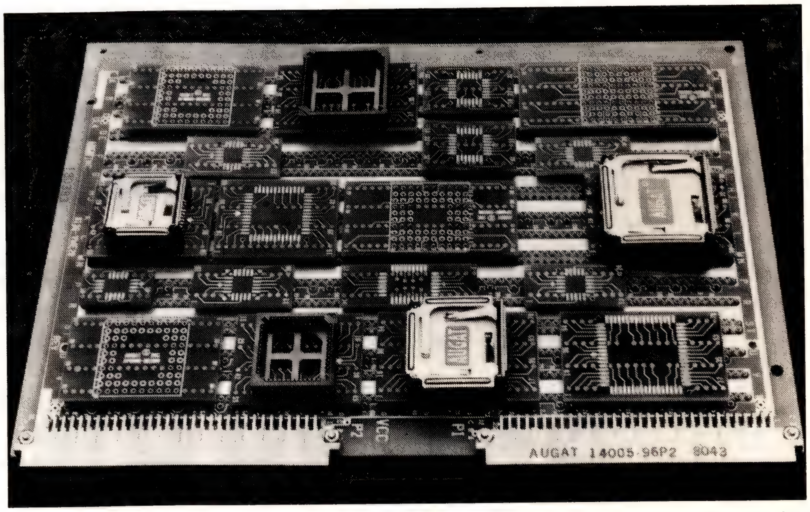
When input/output requirements exceed 100, packaging designers must go to the pin grid array, which is often socketed, or choose from the Japanese plastic quad flat pack or the new bumpered PQFP with gull-wing leads on 25-mil centers [*Electronics*, Oct. 30, 1986, p. 36] recently approved by Jedec. The PGA, a rectangular plastic or ceramic substrate in which a grid of pins are mounted, normally has its pins on 100-mil centers. Molded and glass epoxy sockets for PGAs are readily available.

One new approach to PGA socketing, called the Peel-A-Way system, originally developed by Advanced Interconnections Corp. of West Warwick, R. I., and now used in Augat Inc.'s PKC series of sockets, is based on embedding a PGA pattern of socket terminals in a polyimide film (see fig. 2). The socket terminals are then placed into the pin-grid hole pattern on a pc board and are wave soldered. After the soldering, the polyimide film can easily be removed, resulting in a low-profile PGA socket that is easily inspected.

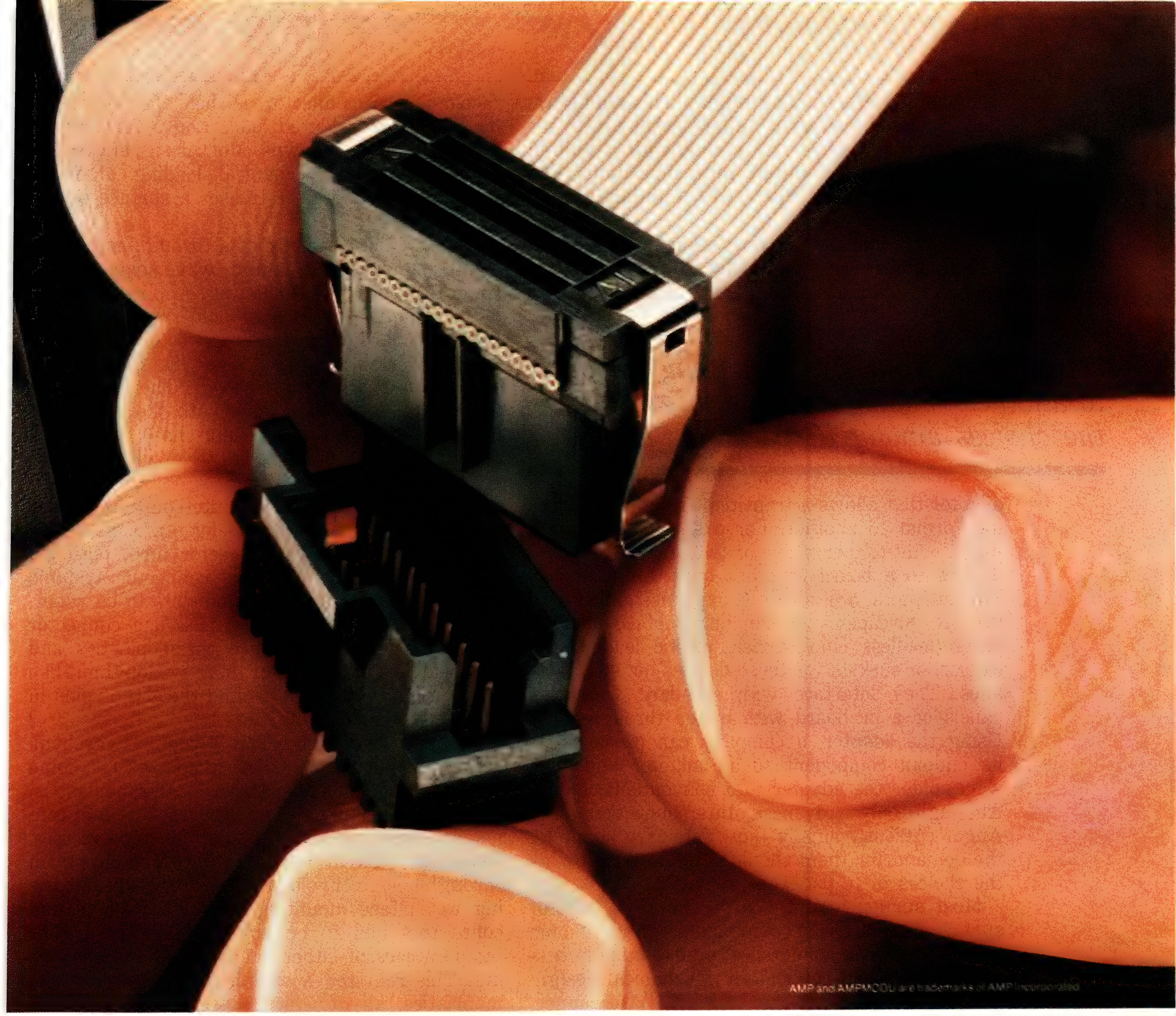
This technique has been extended by both Advanced Interconnections and Augat, of Mansfield, Mass., to include a large sheet of film with pin patterns of either multiple PGAs or a mix of PGAs and DIPs. Customers simply provide either a drawing or computer-aided-design data on their boards, and the pin-bearing film is fabricated allowing all the sockets to be inserted in one operation.

The bumpered PQFP recently approved by Jedec, which has an I/O range of 52 to 244 leads, will have the interconnection density to compete successfully with the PGA. That is why Intel, Motorola, National, and TI are all looking into producing products in this package, and why Amp, Textool, Wells, and Yamaichi are designing production and burn-in sockets for it.

Sockets with integral bypasses are part of a recent trend to take advantage of socket space to enhance performance. Because dynamic random-access memories often must be bypassed or decoupled from their power supplies, this new class of sockets with built-in ceramic bypass capacitors has been developed. The closer the bypass capacitor is to the chip's power leads, the more effective the bypass. DIP sockets with this feature are available from Amp, Augat, and



3. ADAPTERS. A small, leaded adapter board allows nonstandard components to be mounted on standard IC panels or pc boards.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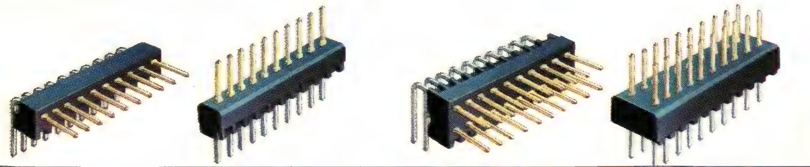

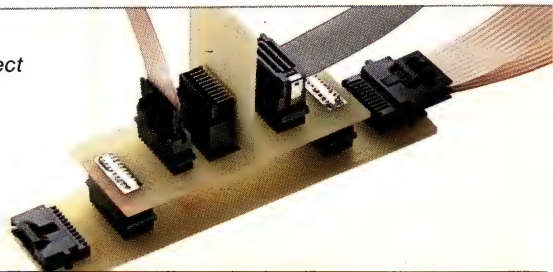

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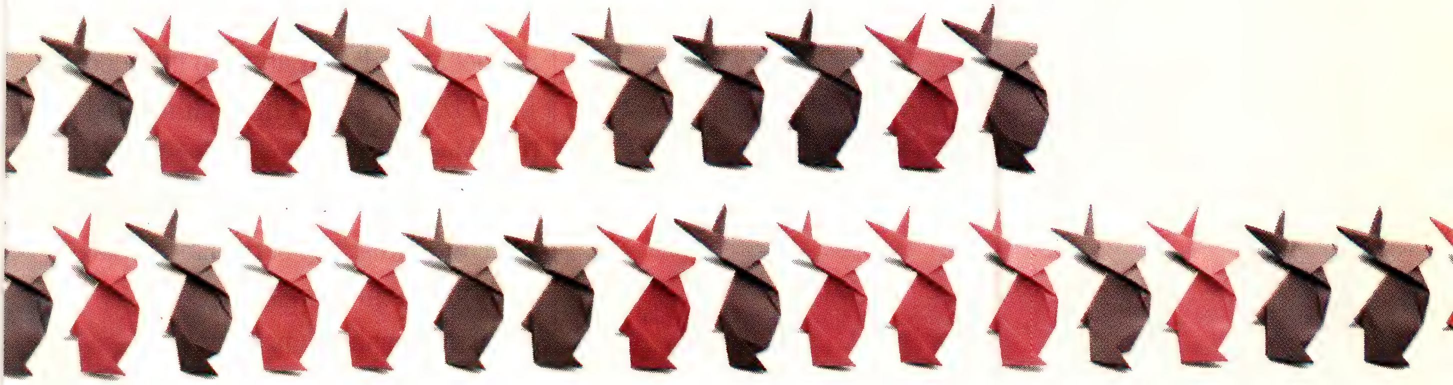

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BIT-SLICE PROGRAMMERS GET A PC-BASED TOOL

Microprogramming the new generation of 32-bit-slice building blocks should get dramatically easier and less expensive. Step Engineering Inc. this month is introducing a $3,695 microprogramming development tool called MicroStep, equivalent in performance to systems costing five times more. What's more, Microstep runs on IBM Personal Computer XTs, ATs, and compatibles; earlier versions of the Sunnyvale, Calif., company's development tool run on dedicated systems, work stations, or minicomputers.

At the heart of the MicroStep system is a high-level microprogramming meta-assembler—called MetaStep, the name of the higher-order language the system uses—that does for bit-slice central-processing-unit development what high-level languages such as C have done for programming on fixed-instruction microprocessors such as the 8086, the 68000, and the more recent 32-bit designs. MetaStep consists of five processor modules and an assembler-to-MetaStep translator (see fig. 1). With a few user-defined high-order language statements, the system programmer using MetaStep can replace several hundred assembly or machine-level statements, says Darrell Wilburn, president of Step Engineering.

The MicroStep product consists of language diskettes, one plug-in card for IBM Corp. Personal Computer ATs or XTs, and one or more interconnection pods to a random-access or read-only memory, or to a programmable ROM. "With this package, the user can turn his IBM XT, AT, or compatible system into a fully functional microcode development system," says Wilburn. "This system is a tremendous breakthrough for the microprogram development marketplace. For years the only tools available were in the $20,000-and-up class. This can open up the market for wider use of microprogrammable components."

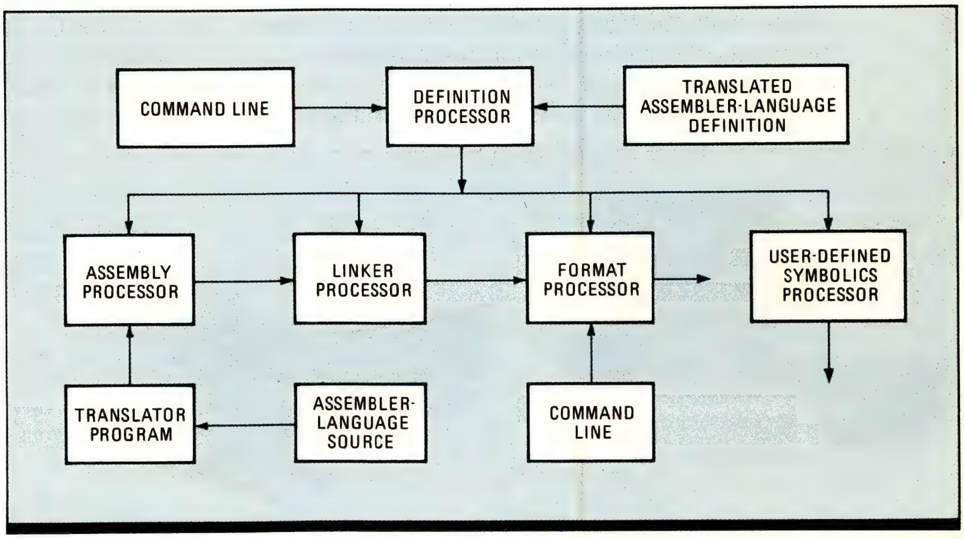
Since the introduction of the language at beta sites late last year, the company has succeeded in expanding the number of systems on which the language is available. In addition to the plug-in board for PC ATs introduced this month and its own PC-AT-based Step 40 microprogramming development system (see fig. 2), MetaStep has also been adapted for use on Digital Equipment Corp.'s VAX minicomputers and Sun Microsystems Inc. work stations.

MicroStep could be widely used in designs with the newer, more powerful microprogrammed 16- and 32-bit arithmetic logic units, and various bit-slice-based building-block digital signal processors, because it simplifies the chore of implementing and debugging large and complicated microcode programs, Wilburn says. An example is the problems a programmer has implementing a common instruction of the 29116, a 16-bit ALU from Advanced Micro Devices Inc.: the subtract with carry, which subtracts data in one location from that in another location and then places the result in a destination while setting the carry bit.

The complication, Wilburn says, arises from the fact that there are many "legal" sources both for the values to be subtracted and for the address of the destination. "Indeed, for this one instruction alone, there are hundreds of possible instruction mnemonic combinations," he says. "Not only are there 12 basic instruction mnemonics to consider, but 32 different RAM register addresses plus three additional instruction mnemonics as well as four non-RAM destinations. That is a total of 396 possible configurations for this single instruction."

To simplify and accelerate the microprogramming of such complex bit-slice architectures, Wilburn and his associates have broken away from the traditional approaches to microprogramming and created, in MetaStep, a language in which the user can create high-level-language-like instructions that are nonpositional in nature; that is, instructions are not dependent on their position in a statement for their effectiveness.

Positional languages involve creating a series of equations that define a name and link an associat-



1. META-ASSEMBLER. Designed for microcode development for 32-bit-slice building blocks, MetaStep consists of five processor modules and an assembler-to-MetaStep translator.

TECHNOLOGY TO WATCH

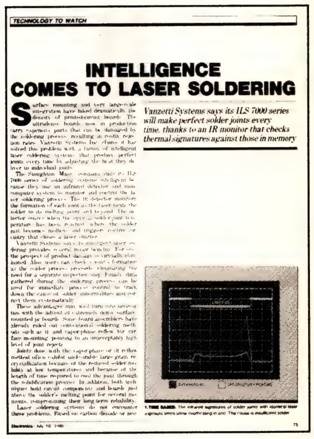
UPDATE: HIGH COST HURTS VANZETTI LASER SOLDERER

A year ago Vanzetti Systems introduced the ILS 7000, an intelligent laser soldering system that offered real advantages over conventional open-loop laser soldering techniques [*Electronics*, July 10, 1986, p. 75]. But despite the promise of the design, the Stoughton, Mass., company has yet to sell one of its ILS 7000 systems.

The intelligent laser solder system contains an infrared monitor that checks solder-joint thermal signatures against a known good joint signature stored in memory. This feedback approach significantly reduces the product damage that often results from conventional systems, while it simultaneously cuts inspection steps and gathers soldering joint data.

The problems selling the system are unrelated to its design, says Dick Alper, director of Vanzetti's system division. The main hindrance to sales has been its cost: the $225,000 price tag on the ILS 7000 is double that of open-loop laser soldering systems. Compounding the problem is the current industry recession, which discourages manufacturers from investing in such relatively expensive equipment.

The company is attempting to reduce the system's cost without compromising its performance. For example, Vanzetti adopted the system's wide-range IR detector from an earlier product, the Laser Inspect system, which is used to inspect finished solder joints. The company now is replacing that detector with a less expensive, uncooled detector that measures the signature of the joint during the soldering process. The ILS 7000 is also being upgraded with improved software and optics. The system can now display thermal signatures in real time instead of printing out the data. Improved optics allow manual observation of laser soldering.


TECHNOLOGY TO WATCH

INTELLIGENCE
COMES TO LASER SOLDERING

Vanzetti Systems says its ILS 7000 series will make perfect solder joints every time, thanks to an IR monitor that checks thermal signatures against those in memory

Electronics/July 10, 1986

75

Two models of the Laser Inspect system have recently been converted in the field to ILS 7000s. One is being used to resolder joints on military pc boards at Texas Instruments Inc. in Dallas. A second is working at Vanzetti's West German office. A third system will reach the field later this year, when Vanzetti upgrades a Laser Inspect system at Siemens AG in Munich. *–Jerry Lyman*

TECHNOLOGY TO WATCH

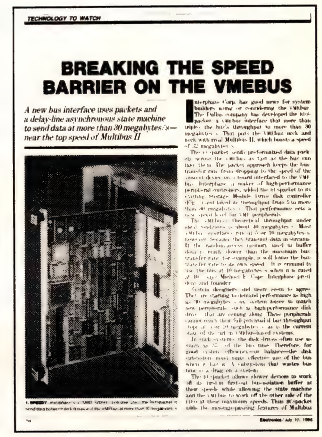
UPDATE: BUS INTERFACE SCORES FOR INTERPHASE

Interphase Corp. is in an enviable position. One year after the Dallas-based company introduced its BUSpacket, a VMEbus interface [*Electronics*, July 10, 1986, p. 58], the competition has not figured out how the design has tripled VMEbus speed to 30 Mbytes/s. Until someone does, Interphase will likely continue to enjoy its 80% share of the VMEbus disk controller market.

"We've had a phenomenal reception," says Michael Cope, Interphase president. "We're winning every benchmark in sight, and BUSpacket is the new standard for speed comparison." The numbers confirm Cope's enthusiasm. The BUSpacket has taken Interphase from $11 million in revenues last year to $15 million today, and the market is leaping ahead at a 60% growth rate. On top of that, Interphase has begun to apply the BUSpacket to other kinds of disk controllers. Meanwhile, competitors have so far only attained bus speeds of 20 Mbytes/s, still 33% slower than the packet design.

To reach its 30 Mbytes/s, the BUSpacket interface formats the data into packets, which are stacked into a 256-word, first-in, first-out buffer, then bursts the information onto the bus as fast as the bus will accommodate it. An asynchronous state machine increases the flow rate between the FIFO and the bus.

Interphase is now leveraging BUSpacket as fast as it can. Already, BUSpacket has spawned a new family of ESDI and SCSI controllers and threatens to influence other architectures, such as high-speed networks operating over Ethernet. The end benefit would be a more efficient use of available bus bandwidths.

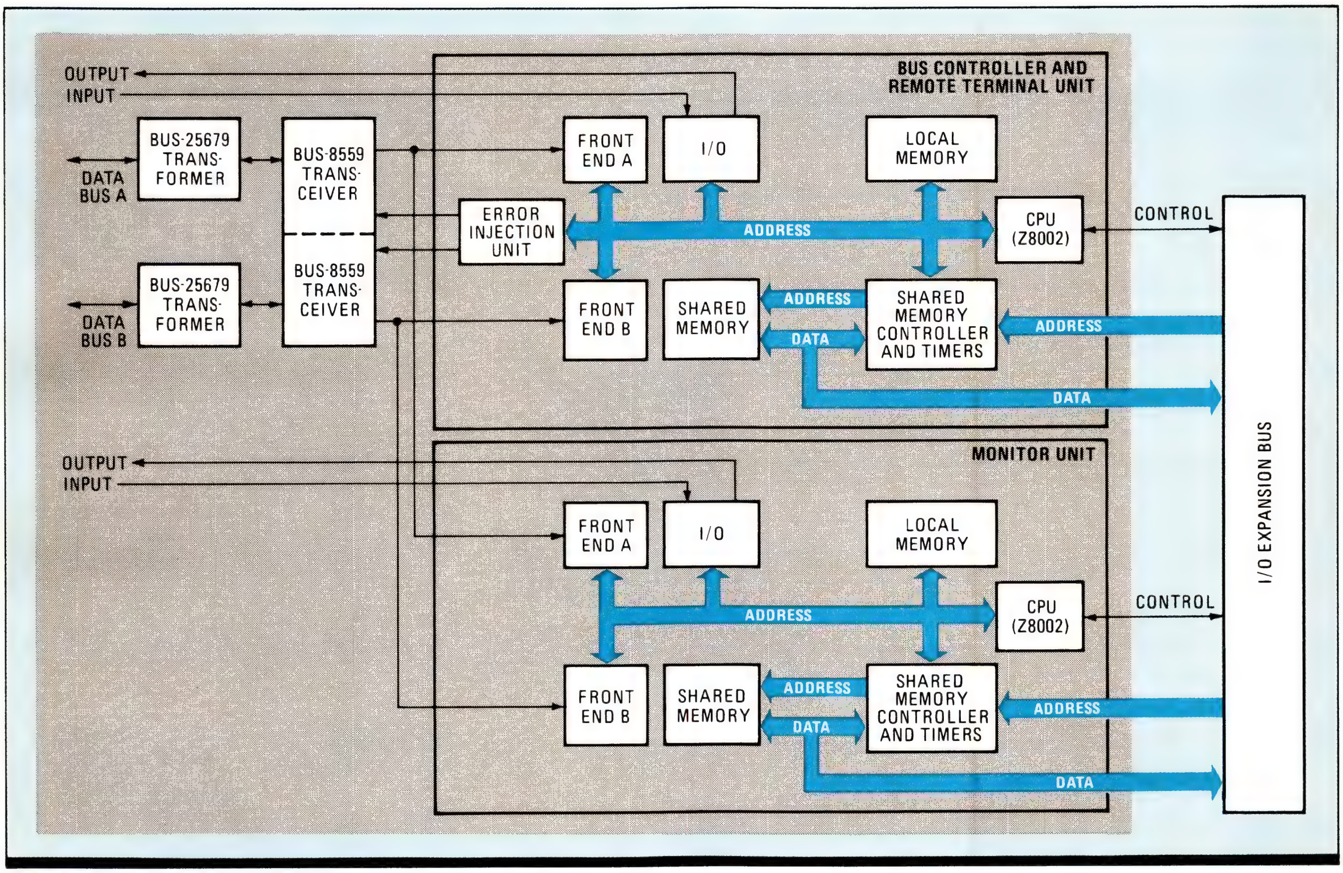

TECHNOLOGY TO WATCH

BREAKING THE SPEED
BARRIER ON THE VMEBUS

A new bus interface uses packets and a delay-line asynchronous state machine to send data at more than 30 megabytes/s—near the top speed of Multibus II

Electronics/July 10, 1986

In the meantime, Interphase plans to continue refining the BUSpacket approach with further degrees of silicon integration and may eventually disseminate the BUSpacket concept through strategic partnerships. Whatever may come, Cope predicts a bright future for VMEbus, thanks to BUSpacket. "Had 10 Mbytes/s remained the top limit for the VMEbus," he says, "that would have opened the door for Multibus II to knock VME out of in-place designs. The VMEbus market share is now protected." *–Stan Runyon*



2. TWO BLOCKS. The dual-redundant 1553B bus enters the board through the transformers and transceivers at the left; the circuitry is then split into two blocks, the bus controller/remote terminal unit block and the monitor unit block, which interface the PC bus.

Each message is assigned a number. All message formats, including broadcast and mode commands, are supported. In addition, a user may specify the type of error to be injected into the message, if any. The error may be an encoding error, a word-length error, or a timing error. The user specifies where the data for the message is to found by indicating which data table is to be used for that message. Data tables may be used by more than one message if desired.

The user defines a frame by filling in a table indicating the order in which the stored messages are to be transmitted. The user may instruct the BUS-65517 to run the frame a specified number of times or to run it until he issues a Halt command.

In the remote-terminal setup mode, the BUS-65517 can simultaneously emulate up to 31 remote terminals. Each terminal maintains its own status and last-command words. The status bits Message Error and Broadcast Busy are determined dynamically.

Each emulated terminal can support 32 sub-addresses for transmitting and receiving. Data tables may be shared between sub-addresses, as well as by multiple remote terminals.

The BUS-65517 automatically handles mode code commands for each individual sub-address. For example, remote terminal No. 4 can be instructed by the bus controller to shut down transmitter A, while the other remote terminals emulated by the board can continue to use that channel. Instructions received on channel A for RT4 will be ignored until an override shutdown-mode code command is received for that terminal.

To define the characteristics of the terminal to be emulated, the user calls up a Setup Remote Terminal menu. This permits the operator to force any bit in the status word to a logic 1 if desired. The user may also define error conditions for the remote terminal. In addition to the basic 1553B errors, the remote terminal can be instructed to respond with the wrong terminal address in its status word, or to suppress the transmission of its status word altogether.

As a Bus Monitor, the BUS-65517 records 1553B transactions. The user may indicate whether to record all messages transferred over a bus or a subset of them, and when to begin recording bus transfers. This is accomplished with a menu whose listings are: Immediate Capture; Command Template—i.e., capture only those messages corresponding to a match between the received command and a template consisting of logical 1s, 0s, and don't cares; error condition detected; and external trigger. The BUS-65517 will detect both word errors and message errors. *–Jerry Lyman*

For more information, circle 485 on the reader service card.

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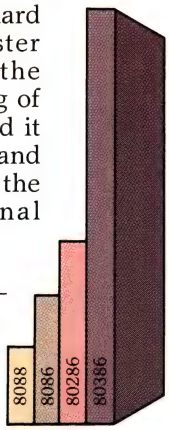

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JULY 9, 1987

MILITARY/AEROSPACE NEWSLETTER

WHY THE ARMY CANCELED RFP FOR ITS LATEST REMOTELY PILOTED VEHICLE

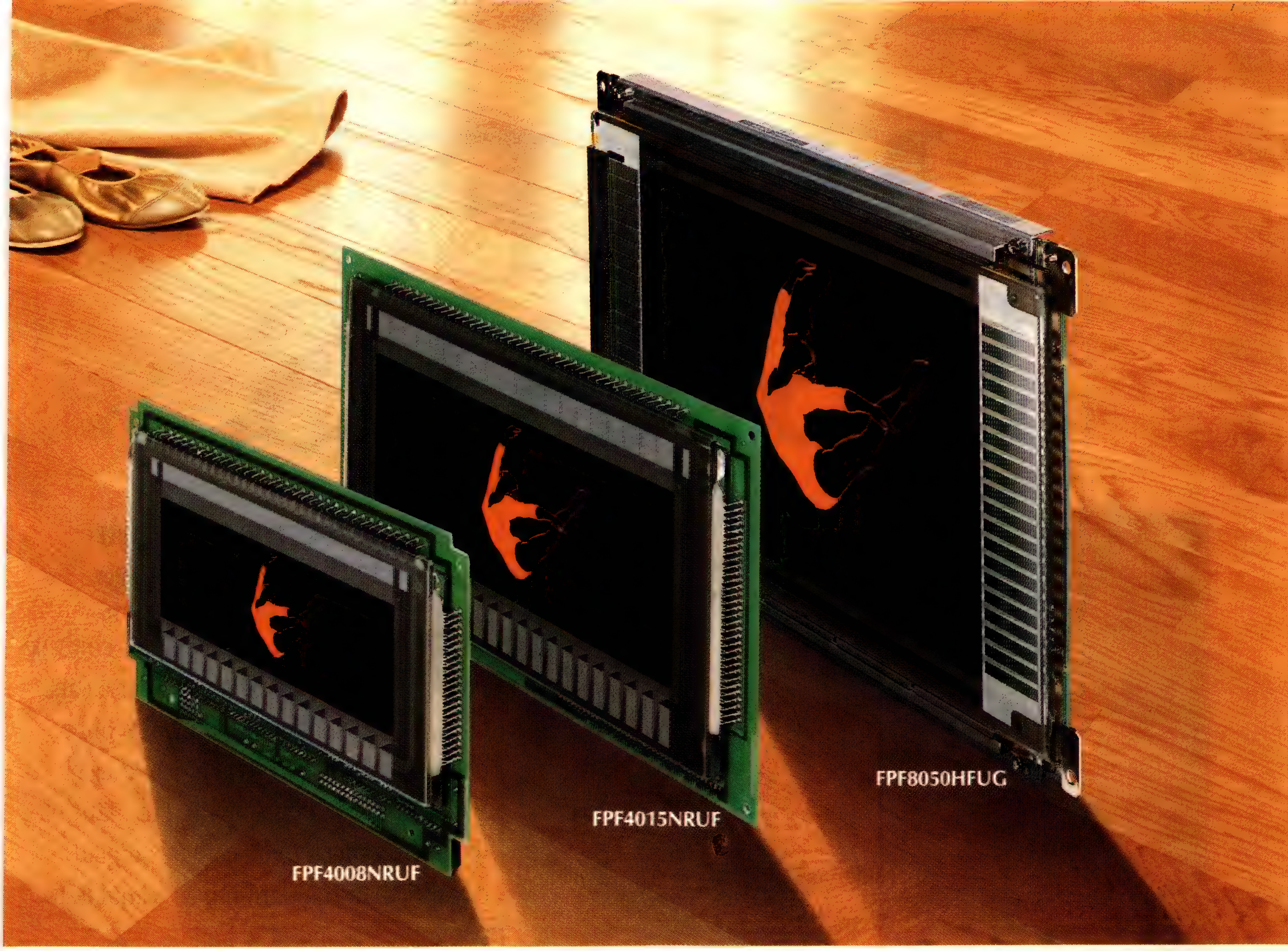
The Army Missile Command, Huntsville, Ala., has notified the two finalists competing for its Intelligence Electronics Warfare/Unmanned Aerial Vehicle contract that it has canceled the current solicitation, and will issue another request for a proposal by the end of August. The companies, California Microwave Inc., Sunnyvale, Calif., and Developmental Sciences, Santa Monica, Calif., got letters saying they didn't meet all requirements of the solicitation. However, a source at one of the firms believes the Navy is thinking about adopting the Army's IEW/UAV for its own long-range reconnaissance operations, and the extension is designed to give the Navy time to review requirements for its remotely piloted vehicle program. The Navy has lost four short-range Pioneer 1 RPVs when they crashed during test flights. The Navy, however, denies any plan to use the Army IEW/UAV. The two finalists, coming off what they thought was a successful competitive fly-off in April, were advised that they will be invited to participate in the next round. The IEW/UAV contract is valued initially at $20 million to $60 million and eventually could be worth $200 million. □

NEW AIR FORCE UNIT WILL OVERSEE LONG-TERM ELECTRONICS R&D

The Electronic Systems Division of the U.S. Air Force's Systems Command is setting up an advanced technology organization that will oversee its programs for the Strategic Defense Initiative, the Air Defense Initiative, and a new Special Projects Directorate. Under a new Deputy Commander for Advanced Techology, the outfit is charged with coming up with concepts and technologies for strategic defense. The new unit is being set up because research for all three projects overlaps to a large extent. The ADI program includes research in surveillance and command and control, with an emphasis on surveillance technologies that could be available in the near term. SDI is studying battle management, which includes command, control, and communications but is oriented toward technologies that will be developed several years from now. The new Special Projects Directorate will concentrate on technologies for advanced surveillance, battle management, and command, control, and communications that could be available in the long term—after the year 2000. The organization will also be responsible for setting up and running the SDI National Test Bed at Falcon Air Station, Colorado Springs, Colo. That facility will be used to simulate key SDI system components. A request for proposals to develop the test bed will be released by the Air Force Systems Command by Sept. 1. □

EVERYONE WANTS TO STUDY SOVIET ELECTRONICS TECHNOLOGY FOR AIR FORCE

When the Air Force Systems Command's Foreign Technology division issued a request for proposals to analyze Soviet electronics technology, it was swamped with responses. So the Wright-Patterson Air Force Base operation has postponed its original June 15 deadline for proposals and is continuing to accept responses from industry. A new deadline has not been set. More than 50 electronics and aerospace companies have already expressed an interest in the fixed-price award. It's a dual contract, meaning the Air Force plans to give the same contract to the two top bidders and presumably will use the best analyses from both studies. The three-year study calls for a review of Soviet systems designs and materials used in the development of electronic countermeasures, ground air-defense and airborne radars, and space-vehicle guidance systems. Also, in mid-July the division will request a synopsis from industry of a one-year study of foreign ballistic missiles and related space systems. The Air Force says teaming will be encouraged for this contract, which should be awarded in the second quarter of 1988. □

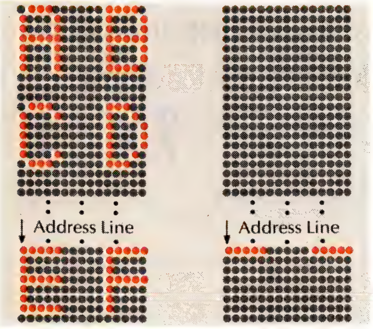


Slim and Trim

The extra-thin plasma displays from Fujitsu

Just 1 inch thick, the new flat-screen plasma displays from Fujitsu are ideal for today's down-sized PCs and OA equipment. Trim down your plasma panels and shape up the quality of your display.

Why Fujitsu's plasma displays are bright and flicker-free?



New Fujitsu memory-type display
All addressed lines light up simultaneously.

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See your data in its best light, thanks to a maximum brightness of 150 cd/m^2.

High resolution:
The FPF8050HFUG's 640 × 400 dot matrix (CRT-compatible) provides crisp displays of graphics and text.

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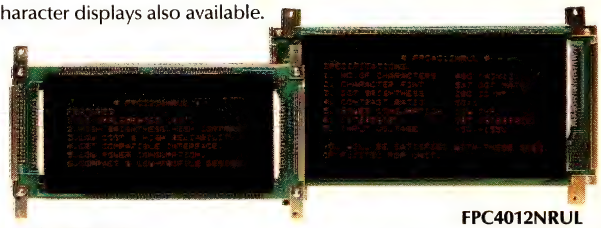
All the drive circuitry is built in. Low consumption minimizes power supply requirements.

Character displays also available.



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Circle 112 on reader service card

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Fujitsu's new FPG-310 plotter is truly compact: it needs only 420 × 260 mm, which leaves you plenty of elbow room. The FPG-310 weighs less than 5 kg and draws less than 35 watts of power.

A wide variety of media

Now you can print figures and text on almost any medium – coated paper, OHP films, tracing paper and, of course, standard paper. And the medium can be any size from postcards to A3 sheets.

Superb graphics

Precise 0.025 mm resolution and 6 bright colors raise your computer's graphics to new heights of effectiveness. The FPG-310 gives you the flexibility of a dot matrix printer but provides far superior quality.

Full compatibility

Three standard interfaces – Centronics, RS-232C and GP-IB – let you connect the plotter to virtually any personal or business computer.

Amazing versatility

Applications include business graphs, education, measurement systems, FA – and even personal CAD. Hobbyists also find the plotter useful for a wide variety of tasks.

Whether you use the FPG-310 in your home office or in a workstation, no job is too big for this little plotter.

Fujitsu Color Plotter FPG-310

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sign size, number of components, or number of layers. The software is available now in prices ranging from $75,000 to $125,000, depending on application and platform. *–Jonah McLeod*

Shared Resources Inc., 2902 Orchard Pkwy., San Jose, Calif. 95134.
Phone (408) 434-0444 [Circle 380]

DSP DEVELOPMENT TIME CUT BY 33%

By providing prefabricated building blocks for the most commonly used digital signal processing functions, Inmos Corp.'s B009/D703 development system for the company's A100 DSP chip cuts as much as a third off application development time.

With code for common DSP functions such as convolutions, discrete Fourier transforms, and finite impulse response filters built in, users can often specify the characteristics of a solution and let the system generate the software.

The B009-1 motherboard containing four A100 chips, 64 Kbytes of random-access memory, and the Inmos T212 transputer plugs into an IBM Corp. Personal Computer or compatible. The optional daughterboard, the B009-2, includes a T414 32-bit transputer with 1 Mbyte of RAM.

Available now, the motherboard costs $4,500. The mother and daughter boards together cost $6,000. The D703 software costs $250. A package of the mother and daughter boards, the D703 software, and the transputer development-system software costs $7,500.

Inmos Corp., P. O. Box 16000, Colorado Springs, Colo. 80935.
Phone (303) 630-4000 [Circle 385]

ANALYZER OFFERS 80 100-MHz CHANNELS

Gould Inc.'s K450B logic analyzer can be configured by keyboard commands to monitor and capture data on up to 80 channels at 100 MHz or across 40 channels at 200 MHz.

Along with a standard 4 Kbytes of memory, the system's performance allows users to analyze state and timing on 32-bit microprocessors without having to relegate some signals to lower speeds because of limitations imposed by the instrument.

The K450B offers a single-key test set-up function for routine analysis applications and a variety of features such as six edge-sensitive and six level-sensitive clock inputs.

Available now, the 80-channel version costs $27,995. A 16-channel version costs $13,795.

Gould Inc., Design & Test Systems Div., 19050 Pruneridge Ave., Cupertino, Calif. 95014. Phone (800) 538-9320 [Circle 386]

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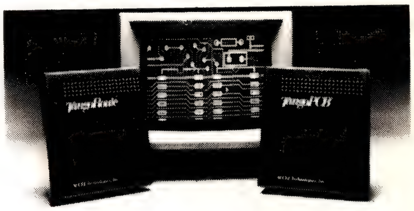

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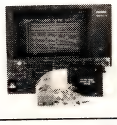

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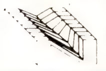

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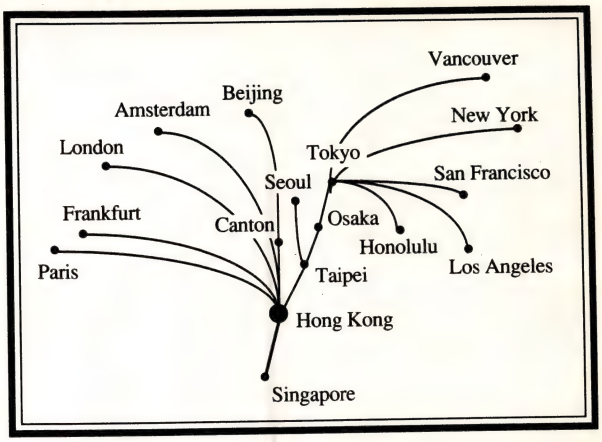

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Colorscan/2 costs $2,000 and volume shipments begin this month. Other storage options include a RAMfile for $750 with 2 Mbytes of internal battery-backed storage, and a cardfile with interface for $150 that handles credit-card-sized non-volatile storage.

Storage devices are treated as MS-DOS disks, and can be used to store and share applications. MS-DOS can be booted from any of the storage options, and the system's connectivity allows users to access and store data in corporate hosts, departmental minis and LAN file servers. *–Lawrence Curran*

Datamedia Corp., 11 Trafalgar Sq., Nashua, N.H. 03063.
Phone (603) 886-1570 [Circle 341]

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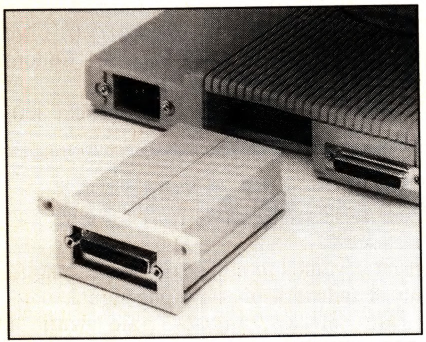
A slot in the keyboard makes that module widely adaptable as well, allowing it to link to any of 14 popular terminals, including Digital Equipment Corp.'s VT 100, 220, and 52 and Wyse Technology's models 50, TV1950, 925, and 910.



The MC10 has three position adjustments—elevation, tilt, and swivel—to accommodate almost any user. Other features are a 720-by-348-pixel display resolution and a 14-in. flat-panel CRT display in green, amber, or soft-white screen phosphors that operates on refresh rates of 60 or 70 Hz.

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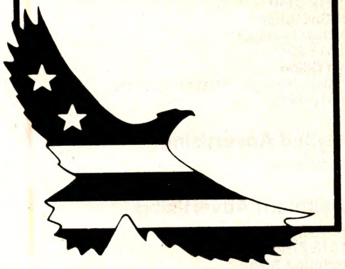

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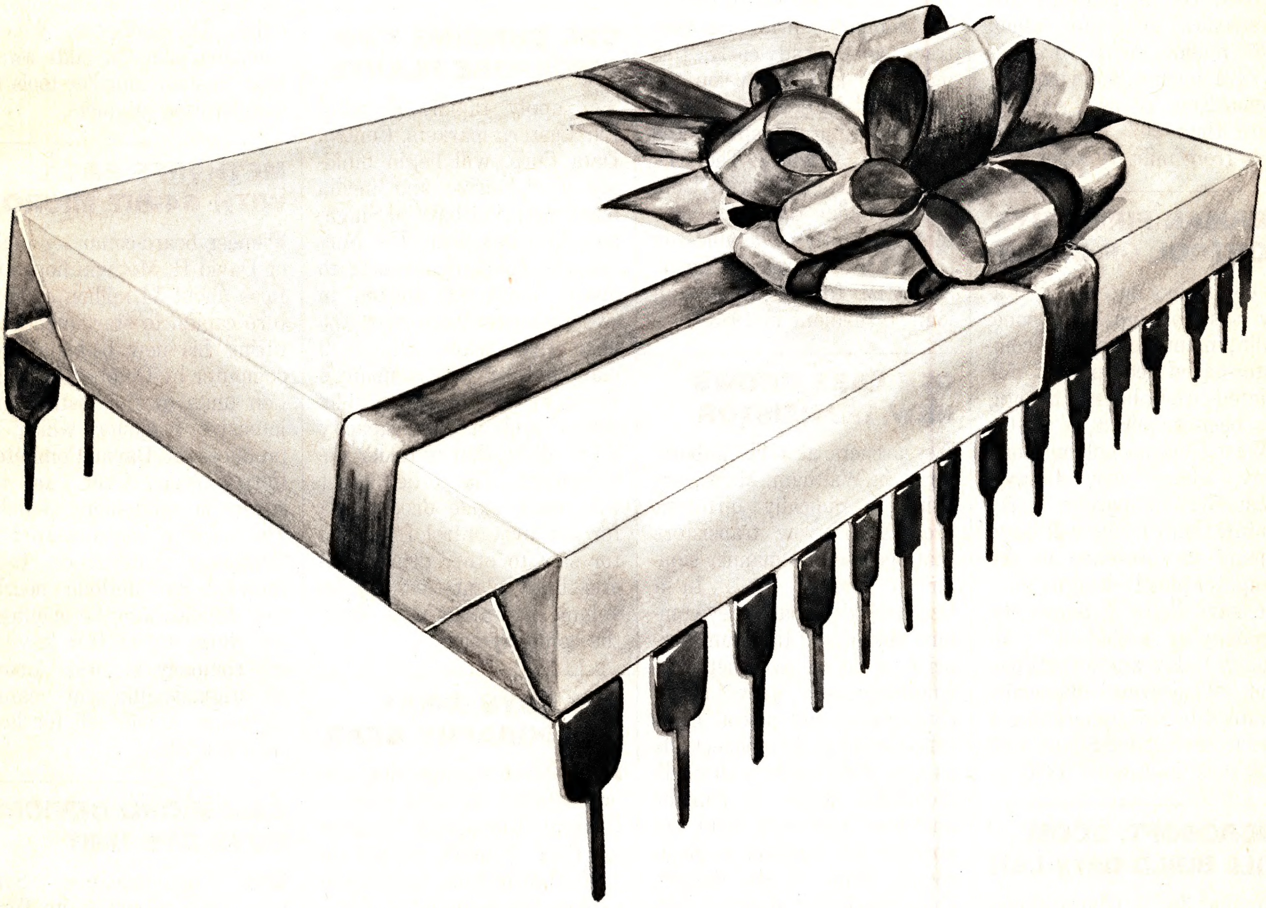

In the August 20th issue, the editors of *Electronics* magazine unwrap a major report on a new generation of VLSI packaging.

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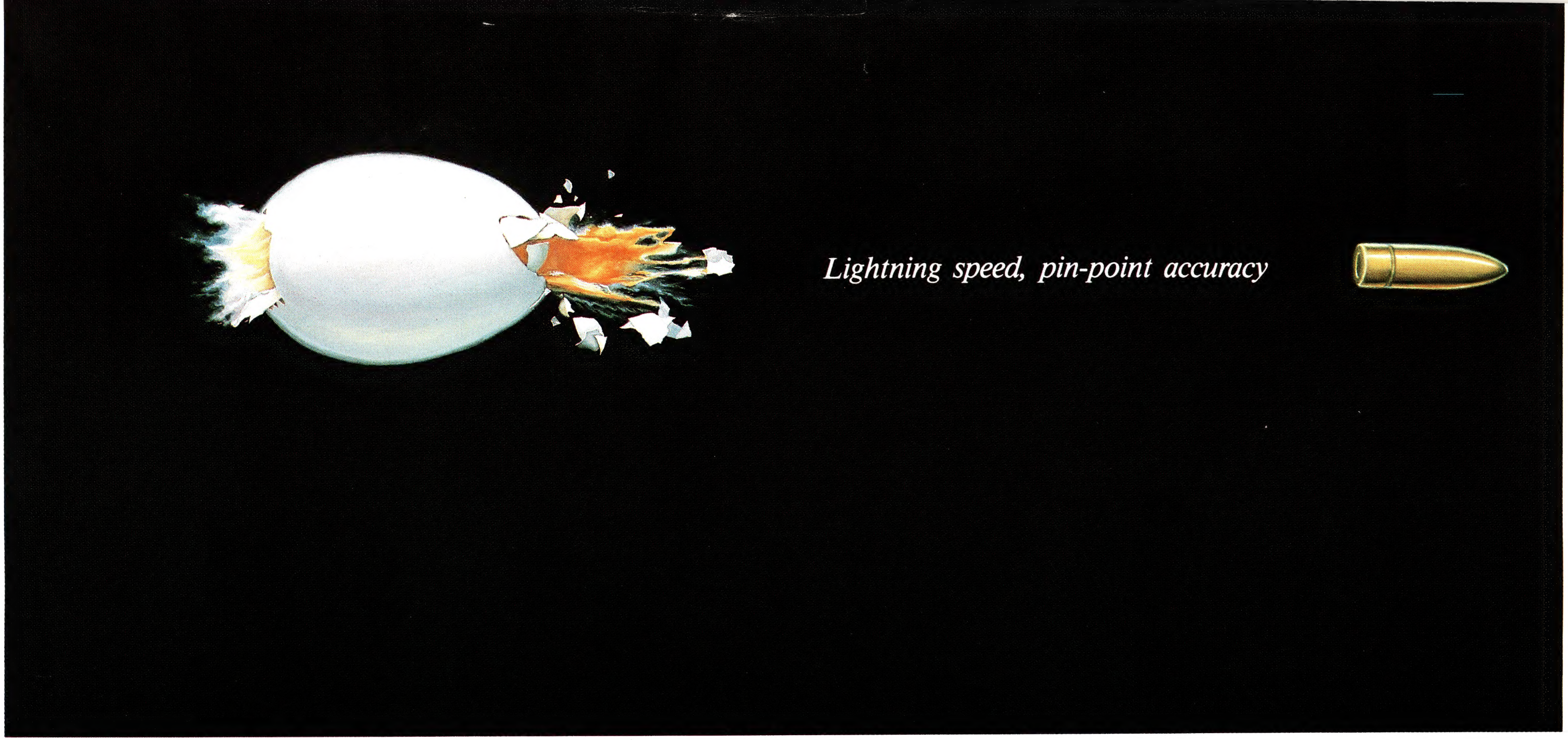

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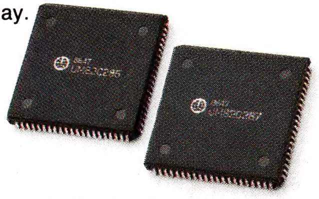

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